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Principal Contributors Stephen Haley Nydia Suarez
Database Coordinator/Graphics & Table Design Fannye Lockley-Jolly
Layout & Text Design Wynnice Napper
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Summary
U.S. beet sugar production for 1998/99 is projected at 4.225 million short tons, raw **value** (STRV), down from 1997/98. The National Agricultural Statistics Service (NASS) has estimated a record sugarbeet crop of 32.66 million tons, but the crop has a poor sugar content.
U.S. cane sugar production for 1998/99 is projected at 3.848 million STRV. Florida is projected at 2.127 million STRV, 10 percent above the preceding record year. Louisiana is projected at 1.260 million STRV, slightly less than last year's record. Texas is projected at 104,402 STRV, a considerable improvement over the previous year. Hawaii is projected at 350,000 STRV, and the Puerto Rico cane sugar is projected at 7,000 STRV.

Imports under the 1998/99 tariff-rate quota (TRQ) are projected at 1.412 million STRV in the May 1999 World Agricultural Supply and Demand Estimates (WASDE) report. Other imports are currently projected at 615,000 STRV, an increase of 120,000 STRV over the April 1999 projection due to an expected increase in imports of high-tier tariff sugar. Other import projections are for the Refined Sugar Re-export Program (175,000 STRV), the Sugar Containing Products Re-export Program (200,000 STRV), imports for the production of polyhydric alcohol (15,000 STRV), and the estimated sugar content of sugar syrups entering the United State s under the tariff heading 1702.90.40 (100,000 STRV).

Deliveries in 1998/99 are currently forecast at 9.975 million STRV. Sugar exports under the Refined Sugar Re-export Program are currently projected at 175,000 STRV. Ending stocks are projected at 1.629 million STRV, resulting in an ending stocks-to-use ratio of 16.0 percent, above the trigger level for the cancellation of the May TRQ tranche.

Beet sugar production for 1999/2000 is projected at 4.530 million STRV, up 7 percent from 1998/99. NASS' estimates of acreage intentions for sugarbeets exceeded last year's acreage planted by 50,000 acres. **Analysis** supports a U.S. yield projection of 21.0 tons per acre, implying a sugarbeet crop of about 31.8 million tons. With normal weather and technical improvements consistent with **historical** trends, sugar yield is projected at 3.00 tons an acre.

U.S. cane sugar production for 1999/2000 is projected at 3.870 million STRV. Florida's cane sugar production is projected at 2.025 million STRV. U.S. cane acreage harvested for sugar is expected to be slightly above this year's level, and sugar per acre is expected to be lower but consistent with trend at 4.71 tons per acre. Louisiana cane sugar production is projected at 1.400 million STRV. Acreage harvested is projected to increase by 20,000 acres, and yields are expected to continue increasing. Texas' cane sugar production is projected at 100,000 STRV, Hawaii's is projected at 330,000 STRV, and Puerto Rico's is projected at 15,000 STRV.

Nonquota imports for 1999/2000 are projected at 725,000 STRV. The largest component is high-tier tariff imports at 260,000 STRV. The remainder of other import projections are for the Refined Sugar Re-export Program (175,000 STRV), the Sugar Containing Products Re-export Program (175,000 STRV), imports for the production of polyhydric alcohol (15,000 STRV), and the estimated sugar content of sugar syrups entering the United State s under the tariff heading 1702.90.40 (100,000 STRV). The raw and refined TRQ for 1999/2000 will be announced later this year but must sum to at least 1.256 million STRV, the World Trade Organization's minimum.

Deliveries for 1999/2000 are projected at 10.150 million STRV, and exports for the Refined Sugar Re-export Program are projected at 175,000 STRV. Projected total use for 1999/2000 sums to 10.325 million STRV, up 175,000 STRV over 1998/99.

The U.S. Department of Agriculture (USDA) currently projects Mexican sugar production for the November 1999/ October 2000 marketing year (MY 1999) at 5.14 million metric tons, raw **value** (MTRV). Acreage is expected to be about the same as this year, although yields should be higher, about 72 metric tons per hectare. Sugar consumption is expected to be flat in MY 1999, about 4.2 million MTRV. Projected exports are 900,000 MTRV, about 6 percent lower than predicted exports in MY 1998. The Mexican Government has agreed to continue its **financing** assistance into MY 1999 to keep stocks at least 600,000 MTRV. Sugar stocks for FY 1999 are projected to be 629,000 MTRV.

U.S. high fructose corn syrup (HFCS) production in 1999 is projected to increase by 4.6 percent to 9.572 million tons: 3.431 million tons for HFCS-42 and 6.141 million tons for HFCS-55. HFCS-42 production growth is projected at 4.1 percent, up from 3.4 percent in 1998. HFCS-55 production growth is projected at 4.9 percent, down from 6.6 percent in 1998.

U.S. Sugar

On May 12, 1999, the U.S. Department of Agriculture (USDA) released

its revised estimate for 1998/99 and its initial projection for 1999/2000.

Current Year, 1998/99

Production

Beet sugar production is projected at 4.225 million short tons, raw **value** (STRV). The National Agricultural Statistics Service (NASS) has estimated the sugarbeet crop at 32.66 million tons, 9.3 percent above the 1997/98 final production estimate.1/

---------- 1/ Unless otherwise noted, sugarcane and sugarbeets are reported in short tons. ----------

Acreage harvested has been forecast at a record 1.452 million acres, 1.6 percent above the previous year. National yield has been forecast at a record 22.5 tons per acre.

Although the size of the sugarbeet crop is a record, it has yielded low sugar content. Based on the estimated sugarbeet yield of 22.5 tons per acre, expected sugar per acre based on the statistical trend would have been 3.12 STRV. However, the actual sugar per acre is projected at 2.91 STRV, nearly 7 percent below expectations. Higher-than-average temperatures have introduced concerns, especially in the Red River Valley region, regarding additional sugar losses stored in piles. USDA **analysis** concludes that, while there has been some pile deterioration due to the unseasonably high temperatures, most beets have survived the winter intact, allaying concerns of further reductions in beet sugar projections. The slicing campaign in the Red River Valley is still expected to run through June. The California campaign has started, and sugar production from the desugaring of molasses and from thick juice stored during the slicing campaign in other regions will contribute to production for the remainder of the year.

Cane sugar production is projected at 3.848 million STRV.

Campaigns in Florida, Texas, and Louisiana have ended, implying mainland production of 3.491 million STRV. Production will continue for the remainder of the year in Hawaii and will start soon in Puerto Rico.

Florida cane sugar is projected at 2.127 million STRV. Current year production is projected over 10 percent above the preceding year, which was a record. NASS has estimated the sugarcane for sugar crop at 16.860 million tons on 429,000 acres. Sugar is projected at a record 4.96 tons, 8.5 percent above the preceding year. Growers benefitted from dry and very warm conditions throughout the growing season. Irrigation and effective management practices helped mitigate against drought conditions that affected other Florida crops. Because of the large sugarcane crop, the season ran 3 weeks longer than normal into the latter part of April.

Louisiana cane sugar is projected at 1.260 million STRV. This year's total is slightly less than last year's record but is the second highest for the State. NASS has estimated the sugarcane for sugar crop at 11.6 million tons on 400,000 acres. Sugar per acre is projected at 3.15 tons, down 5 percent from the previous year's record 3.32 tons per acre. The region experienced very dry and hot conditions through most of the growing season and received drenching rain in the fall as several tropical storms passed through. Wet conditions pushed back the harvest, which was not completed until several weeks into January. Although individual growers may have experienced some losses, sources indicate that the cold tolerance of current sugarcane varieties helped the crop survive January conditions. Moreover, the sugarcane variety LCP85-384 has sparked a yield-enhancing revolution, which has produced the heavier sugar content.

Investments in new chopper harvesters have been made at the same time, helping to mitigate lodging problems that can result with heavier cane.

Texas cane sugar is projected at 104,402 STRV, a considerable improvement over the previous year's 79,569 STRV. The Texas producing area suffered through drought conditions for most of the season, but plentiful rain occurring in the fall contributed to increased sugarcane development. Although there had been some question regarding sugar content, results indicate that sugar tonnage per acre netted 3.26, up nearly 10 percent over

the previous year. The milling season extended until the middle of April.

Hawaii cane sugar is projected at 350,000 STRV. NASS does not forecast 1999 sugarcane acreage until June. However, local analysts conservatively forecast this year's sugar production to equal the previous year's 350,000 STRV. Through March, the fiscal year production has totaled 95,700 STRV, about 96 percent of the previous year through the same period. One source of concern has been the Pioneer mill on Maui. High costs have forced the owner (AMFAC/JMB Hawaii) to discontinue sugar production at the end of the season in September.

Puerto Rico cane sugar is projected at 7,000 STRV. This low projection takes into account hurricane damage that put the Roig mill out of operation for this year. The only other mill, Central Agraso (formerly Coloso), will account for total Puerto Rican production this year.

Imports

Imports under the tariff-rate quota (TRQ) are projected at 1.412 million STRV in the May 1999 World Agricultural Supply and Demand Estimates (WASDE) report. This amount reflects the cancellation of January and March tranches (165,345 STRV each) that resulted when the ending stocks-to-use projections published in the WASDE for those months were above 15.5 percent. The cancellation of the May tranche, due to a projected ending stocks-to-use ratio of 16.0, is not reflected. The cancellation of the May tranche implies a downward revision of imports under the TRQ by 165,345 STRV.

Other imports are currently projected at 615,000 STRV, up 120,000 STRV over the April 1999 projection. The projection of high-tier tariff sugar entering from Mexico caused the increase. Through April 1999, about 184 STRV high-tier tariff Mexican sugar had entered the United States. In May 1999, raw sugar amounting to about 15,432 STRV entered. Data available to USDA indicate that additional tonnage sufficient to bring the total to 120,000 STRV for the year now awaits entry. The incentive for traders to deliver high-tier tariff Mexican sugar into the United States is explained by several factors: low world prices below 6 cents a pound (No. 11 CSCE Contract, New York), a high-tier tariff rate for raw and refined sugar under the North American Free Trade Agreement (NAFTA) of 13.6 cents a pound and 14.42 cents a pound, and the absence of price-based safeguards that apply to over-quota sugar from all sources except Mexico and Canada.

The remainder of other import projections are for the Refined Sugar Re-export Program (175,000 STRV), the Sugar Containing Products Re-export Program (200,000 STRV), imports for the production of polyhydric alcohol (15,000 STRV), and the estimated sugar content of sugar syrups entering the United States under the tariff heading 1702.90.4000 (100,000 STRV).

Deliveries, Exports, and Stocks

Total deliveries, including deliveries for human consumption, sugar included in products for the Sugar Containing Products Re-export Program, deliveries for use in the Polyhydric Alcohol Program, and for feed use are currently forecast at 9.975 million STRV. Exports of sugar under the Refined Sugar Re-Export Program are currently projected at 175,000 STRV. Ending-period 1998/99 stocks are calculated as a residual of total supply (projected 11.779 million STRV) less total use (projected 10.150 million STRV). Ending stocks are, therefore, projected at 1.629 million STRV. The projected stocks-to-use ratio is 16.0 percent, above the trigger level for the cancellation of the May TRQ tranche.

Prices

U.S. raw sugar prices (nearby futures, C.I.F., duty-paid, Contract No. 14, New York) averaged 22.57 cents per pound during April, up just 2 points from the March average. The range for the month was 66 points, from a high of 22.98 on April 1 to a low of 22.32 on April 23, before closing on the 30th at 22.65 cents per pound. July No. 14 futures prices averaged 22.48 cents in the first 8 market days of May, with a maximum and a minimum price of 22.70 cents and of 22.27 cents per pound. Increasing U.S. sugar deliveries and the outlook for lower 1999/2000 U.S. sugar carryover stocks may have boosted nearby futures prices recently. Wholesale refined beet

sugar prices (F.O.B. plant, Midwest markets) have come down 0.20 cents to 27.00 cents a pound in April, likely reflecting the pressure of a larger 1999 crop.

World raw sugar prices, which have been in steady decline over the past year, bottomed out during the last week of April when the July contract traded as low as 3.93 cents per pound on April 28, a 14-year low. The bargain basement prices have attracted buying from Bangladesh and Iran, and interest from potential Russian buyers. Prices firmed somewhat at the end of the month when the July contract closed at 4.33 cents. Part of the reason for the firmer prices were the shipping delays at two major Brazilian ports. However, the outlook remains negative as bumper crops in major exporting countries continue to be met with weak demand. World raw sugar prices averaged 5.44 cents a pound in April, compared with 10.22 cents in the same month a year earlier.

Forecasts for 1999/2000

Production

Beet sugar production is projected at 4.530 million STRV, an increase of over 7 percent from 1998/99. NASS estimates of acreage intentions for sugarbeets by State sum to 1.548 million acres, exceeding last year's acreage planted by 50,000. Although NASS does not forecast acreage harvested until June, **historically**-based ratios between acreage harvested and acreage intentions by State support an early-season projection of 1.510 million acres for the United States. **Analysis** of State-level yields supports a U.S. yield projection of 21.0 tons per acre, implying a sugarbeet crop of about 31.8 million tons. With normal weather and technical improvements consistent with **historical** trend, sugar yield is projected at 3.00 tons an acre, implying total production of 4.530 million STRV. The sugar recovery rate is projected at 14.23 percent, nearly 10 percent above the projected rate for 1998/99, but below the rates for 1996/97 (15.04 percent) and 1997/98 (14.69 percent).

Cane sugar production is projected at 3.870 million STRV, slightly above the projected total for 1998/99. This total reflects expectations regarding production from Florida, Louisiana, Texas, Hawaii, and Puerto Rico.

Florida cane sugar production is projected at 2.025 million STRV, down from this year's projected record, but it would still be the second highest in the State's production history. Cane acreage harvested for sugar is expected to be slightly above this year's level at 430,000 acres. Sugar per acre is expected to be down but consistent with trend at 4.71 tons.

The mix of sugarcane varieties used in Florida is very well suited to local conditions. Irrigation in muck soils helps considerably in safeguarding the crop from drought conditions that cause havoc to other crops. Good management practices by growers and processors contribute as well. A structural upward shift in cane yields was evidenced in 1997/98. High cane yields continued in 1998/99 and are projected at 38.2 tons an acre in 1999/2000. The cane crop is projected at 16.4 million tons, slightly lower than last year's crop. Sucrose recovery is projected at 12.33 percent, or about 247 pounds per ton of cane.

Louisiana cane sugar production is projected at 1.400 million STRV, up 11 percent from 1998/99. Acreage harvested is projected to increase by 20,000 acres over 1998/99 to 420,000 acres. The expected expansion is centered in the northern cane region where alternative crop prices have made the growing of sugarcane a much higher-valued alternative in spite of long trucking distances from mills. The continued expansion of the LCP85-384 sugarcane variety implies less of a percentage of sugarcane land in fallow: about 20 percent instead of the usual 25 percent. This results because the LCP85-384 permits a third stubble crop, thereby keeping more land in production.

Increased acreage planted to the LCP85-384 has increased Louisiana cane yields above earlier trends. With LCP85-384's share of sugarcane acreage increasing to about 60 percent, cane and sugar yields are expected

to increase as well. The projected cane yield is 29.5 tons per acre, up 0.5 ton over 1998/99. The projected sugar yield is 3.33 tons per acre, up 0.18 ton an acre from the year before.

Texas cane sugar production is projected at 100,000 STRV.

Projected acreage harvested of cane for sugar is 32.0, the same as 1998/99. Projected cane yield of 31.25 tons per acre is lower than 1998/99, however, because there is less acreage devoted to the cane crop. Sugarcane is projected at 1.0 million tons. Under normal conditions, an expected recovery rate of 10 percent would imply the 100,000 STRV production level. One concern, however, is that the current dry conditions resemble the extremely dry spring of a year ago.

Hawaii cane sugar production is projected at 330,000 STRV. The key factor for Hawaii is the closing of the Pioneer Mill in Maui. This mill has produced about 20,000 to 25,000 in the mid- to late-1990s. A reduction of 20,000 STRV from the 1998/99 forecasted 350,000 STRV is the basis of the 1999/2000 Hawaii projection. A forecasting difficulty with respect to Hawaii is that the 1999 NASS forecasts of Hawaii acreage and production relate to 1998/99 rather than 1999/2000. The first NASS acreage forecast for 1999/2000 will not come until June 2000.

Puerto Rico cane sugar production is projected at 15,000 STRV. The reconstructed Roig mill should be back in operation, which should put production back to levels in 1997/98. Nonetheless, the Puerto Rican sugar sector still faces high costs and problems stemming in part from the privatization of the mills.

Imports

Non-TRQ imports for 1999/2000 are projected at 725,000 STRV. The largest component of non-TRQ imports are imports entering at the high tariff. Most of these imports are expected to be sourced from Mexico. The NAFTA high-tier tariff for raw sugar (96 pol) is reduced from 13.60 cents a pound to 12.09 cents a pound in calendar 2000. The corresponding tariff for refined sugar (100 pol) is reduced from 14.42 cents a pound to 12.81 cents a pound. There are no price-based safeguards for sugar sourced from NAFTA countries, and world prices are expected to remain at low levels for the foreseeable future. It is probable that incentives for traders to import high-tariff Mexican sugar will be limited by the effect it has on the No.14 Contract raw sugar futures price. It is probable that the most important effect of increased Mexican imports will be to reduce the TRQ.

The remainder of other import projections are for the Refined Sugar Re-export Program (175,000 STRV), the Sugar Containing Products Re-export Program (175,000 STRV), imports for the production of polyhydric alcohol (15,000 STRV), and the estimated sugar content of sugar syrups entering the United States under the tariff heading 1702.90.40 (100,000 STRV). The raw and refined TRQ for 1999/2000 will be announced later this year but must sum to at least 1.256 million tons.

Deliveries and Exports

Total deliveries are projected at 10.150 million STRV, an 1.8-percent increase over the previous year. Total deliveries include sugar included in products for the Sugar Containing Products Re-export Program (175,000 STRV), deliveries for use in the Polyhydric Alcohol Program (15,000 STRV), and for feed use (7,000 STRV). Deliveries for human consumption are calculated as a residual: 9.953 million STRV. Additionally, exports for the Refined Sugar Re-export Program are projected at 175,000 STRV. Projected total use for 1999/2000 sums to 10.325 million STRV, a growth of 175,000 STRV over 1998/99.

Deliveries to industrial users are projected to increase by 2.5 percent, while deliveries to non-industrial users are projected to increase by only 0.8 percent. The share of industrial users' deliveries is projected to grow to 59.6 percent in 1999/2000, up from 59.2 percent forecast for 1998/99. Deliveries to confectioners, although down the first half of 1998/99 by over 4 percent compared with a year ago, are expected to recover. Deliveries for baking and cereal uses and for multiple uses are expected to continue their strong trend growth patterns.

Mexican Sugar

The U.S. Department of Agriculture (USDA) currently projects Mexican sugar production for the November 1998/October 1999 marketing year (MY 1998) at 5.04 million metric tons, raw **value** (MTRV). The Mexican Government's sugar agency, Coaazucar, pegs production in its fourth sugar estimate somewhat lower, at 4.705 MTRV. Regardless of source, it is agreed that production is down from the previous year due to decreased yields resulting from extremely dry weather throughout most of the growing season. Also, the harvest season in Veracruz was delayed by excessively wet weather just prior to the normal harvest starting date. Labor shortages contributed to harvest problems in the states of Veracruz, Tamaulipas, and San Luis Potosi. Sugar consumption is projected at 4.24 million MTRV, with the soft drink industry demanding between 1.2 to 1.4 million MTRV. Sugar exports are projected at 955,000 MTRV. The Mexican Government helps to **finance** storage costs up to 600,000 MTRV. Ending stocks are projected at 759,000 MTRV.

USDA currently projects Mexican sugar production for MY 1999 at 5.14 million MTRV. Acreage is expected to be about the same as this year, although yields should be higher, about 72 metric tons per hectare, assuming normal weather patterns. Producers are reportedly holding high inventories, and with low export prices, producers are not planning for major expansions next year. Sugar consumption is expected to be flat in MY 1999, about 4.2 million MTRV. Producers claim that stagnant demand growth is attributable to the replacement of sugar by imported and domestically-produced high fructose corn syrup. Although soft drink demand is expected to grow by 3 percent next year, most of the growth is in bottled water and diet products. Projected exports are 900,000 MTRV, about 6 percent lower than predicted exports in MY 1998. The Mexican Government has agreed to continue into MY 1999 its **financing** assistance in keeping stocks at least 600,000 MTRV. Sugar stocks for FY 1999 are projected to be 629,000 MTRV.

In January 1999, negotiations between sugarcane producers, the Mexican Government, and the sugar industry produced an agreement that pays growers 57 percent of the wholesale reference price for a metric ton (mt) of standard sugar. The price was increased to 3,688.42 pesos per mt, FOB mill, or US$368.84 per mt. Growers receive 2,102 pesos per mt, up 5 percent from MY 1997. The reference price for MY 1999 will be 3,921.96 pesos per mt.

High Fructose Corn Syrup

The combined production of high fructose corn syrup (HFCS) for 1998 is estimated at 9.15 million short tons, dry weight, 5.5 percent above 1997. 1/

--------- 1/ Throughout this report, high fructose corn syrup is reported in short tons, dry basis, unless otherwise noted. ---------

HFCS-42 production is estimated to comprise about 36 percent of the total, or 3.296 million tons. The remainder (5.854 million tons) is comprised of HFCS-55 syrup. 2/

-------- 2/ In this report, the HFCS-55 comprises corn sweetener products whose fructose composition is 55 percent or higher. These products include HFCS-55 syrup, HFCS-55 solid, HFCS-90, crystalline fructose, and others. --------

Domestic deliveries of HFCS-42 grew by only 3.4 percent to 3.318 million tons. HFCS-55 deliveries grew by 5.1 percent to 5.561 million tons. HFCS-42 exports were small (39,000 tons), and were less than imports (61,000 tons). HFCS-55 exports grew by 36 percent to 349,000 tons and now comprise 5.9 percent of total estimated use, up from 3.7 and 4.6 percent in 1996 and 1997.

HFCS production in 1999 is projected to increase by 4.6 percent to 9.572 million tons: 3.431 million tons for HFCS-42 and 6.141 million tons for HFCS-55. HFCS-42 production growth is projected at 4.1 percent, up from 3.4 percent in 1998. HFCS-55 production growth is projected at 4.9 percent, down from 6.6 percent in 1998. Actual first-quarter (January-March) data

show strong HFCS-42 deliveries of 10.4 percent growth over the same period last year. Comparable first-quarter HFCS-55 deliveries, on the other hand, were only 1.7 percent, which compares with 3.8 percent growth for the first quarter of 1998--less than half as much. For the entire year, HFCS-42 domestic deliveries are projected at 3.436 million tons, representing 3.6 percent yearly growth. HFCS-55 domestic deliveries are projected at 5.756 million tons, representing 3.5 percent yearly growth, down from 5.1 percent for 1998.

Exports are difficult to project but should continue to expand. Figure 1 shows HFCS-55 exports since 1996 to both Mexico and the world. Total exports have grown from 190,000 tons in 1996, to 257,000 tons in 1997, and 349,000 tons in 1998. In 1996, exports to Mexico comprised 71 percent of the total. Although exports to Mexico have continued to expand (153,000 tons in 1997 and 178,000 tons in 1998 according to U.S. Customs data), their proportion of total exports has declined: 60 percent in 1997 and 51 percent in 1998. With increased compensatory duties on U.S. Mexican exports (see below), export growth to Mexico will likely decrease (although January and February U.S. export data show the opposite). However, if trends to other importers continue, U.S. HFCS-55 exports should continue to grow despite a slowdown to Mexico. The current 1999 export projection is 429,000 tons, up 23 percent over 1998.

Milling and Baking News reports some moderate strengthening of HFCS-42 spot prices. They were at a low of 9.9 cents a pound in the third quarter of 1998 but have risen to 11.33 cents a pound in the first quarter of 1999. Even so, the 1999 first-quarter average is below the comparable period for 1998, when the spot price averaged 11.53 cents a pound.

Figure 2 shows the ratio of the HFCS-42 spot price to the Midwest wholesale beet sugar price, also reported in the Milling and Baking News. Although beet sugar prices have recently risen over 1998 levels, the HFCS-42 spot price has increased proportionally more, thereby causing the ratio of the two prices to rise to 0.42 from a low of 0.38 in the third quarter of 1998. A 0.42-ratio level is still low by **historical** standards: the ratio averaged 0.61 in 1995 and 0.50 in 1996 before dropping precipitously in 1997. Although the U.S. Department of Agriculture (USDA) does not project HFCS prices, it would not seem likely that HFCS prices will return this year to the high levels achieved 3 and 4 years ago. The U.S. HFCS sector is still burdened by excess capacity, and it will take some time for demand to catch up with existing supply potential.

Figure 3 shows net corn cost relative to the spot HFCS-42 price. The ratio fell below 0.30 in the third quarter and averaged 0.25 in the first quarter of 1999. From a cost perspective, HFCS producers would seem much better off relative to 1996, 1997, and even 1998. Although difficult to predict, net corn costs are not likely to vary much in 1999. USDA reports that 1999 intended corn acreage is down 2 percent, but weak feed demand will likely limit any upward price movements implied by reduced production.

Byproduct prices (mainly corn gluten meal and feed) that offset the cost component of corn prices are at **historically** low levels and are likely to remain there.

HFCS and Mexico

There are two HFCS producing facilities in Mexico. ALMEX is located in the state of Guadalajara and is jointly owned and operated by A.E. Staley Manufacturing Company and Archer Daniels Midland. ARANCIA is located in the state of Queretaro, and Corn Products International, Inc. now has a controlling interest. Corn used in wet milling is imported into Mexico from the United States under a tariff-rate quota (TRQ) administered by the Mexican Secretariat of Commerce and Industrial Development (SECOFI). The TRQ for 1998 was 1,622,032 metric tons (mt), and 432,410 mt for the first quarter of 1999. Although there is no available public data, sources indicate that domestic HFCS production was between 220,000 and 300,000 mt in 1998. Output is not expected to expand significantly in 1999. Sources also indicate that domestic HFCS production displaced between 170,000 and 230,000 mt of sugar consumption in Mexico in 1998.

Presumably, this same level of displacement would be expected in 1999 as well.

HFCS imports from the United States face compensatory duties. The duties were applied by SECOFI in June 1997 when SECOFI alleged that HFCS was being dumped into the Mexican market. These duties were made permanent in January 1998 when the dumping allegations were substantiated. Duties were also imposed on HFCS-90 in September 1998 after SECOFI concluded that HFCS-90 was being imported in order to avoid previously-imposed duties on HFCS-55. (Because HFCS-90 is used by HFCS-producing facilities in Mexico to produce HFCS-55, the duties help to limit domestic HFCS production.) Table T-x shows compensatory duties by product and company.

In February 1998, the U.S. Corn Refiners' Association (CRA) asked for a dispute settlement under the North American Free Trade Agreement (NAFTA) to review the duties. By late 1998, the five members had been named to the NAFTA panel. The panel will commence to review legal briefs submitted by the CRA and SECOFI in 1999. Parallel to actions undertaken for NAFTA, the United States Trade Representative (USTR) announced its intention on May 8, 1998, to invoke World Trade Organization (WTO) dispute settlement proceedings. The USTR has made two formal requests for the formation of a WTO panel. The first request was blocked by Mexico. The second request was made on November 25, 1998, and could not be blocked by Mexico. Progress in the WTO is expected to be slow.

In May 1998, the USTR initiated an investigation under section 302 of the Trade Act of 1974, as amended (the Trade Act), in response to a petition by the CRA, alleging that the Government of Mexico had denied fair and equitable market opportunities to U.S. HFCS exporters. The CRA argued that the Mexican Government had encouraged and supported an agreement between representatives of the Mexican sugar industry and Mexican soft drink bottling industry to limit purchases of HFCS by the soft drink bottling industry. On May 15, 1999, the USTR concluded its formal investigation phase as required by the terms of the section 302 statute without determining legally that the Mexican Government's alleged practices were actionable under section 301 of the Trade Act. However, the USTR noted that its investigation had raised enough questions about the actions of the Mexican Government to warrant further examination and continued consultation with the Mexican Government on issues related to trade in HFCS.

In December 1998, the United States dropped a safeguard measure meant to protect the U.S. broomcorn broom industry from Mexican imports. As a result, Mexico dropped its retaliatory duties that had been put in place on U.S. HFCS imports as well as other U.S. agricultural imports. As a result, the 12.5 percent ad-valorem duty was reduced to the NAFTA-specified rate of 6 percent.

Level of U.S.-Mexico HFCS-55 and HFCS-90 Trade

One issue that complicates trade discussions with Mexico is the uncertainty with regard to the level of U.S. HFCS shipments to Mexico. Exports reported by the U.S. Customs Service do not correspond to those reported by SECOFI. Figure H4 shows HFCS-55 and higher shipments as reported by both sources, along with the corresponding tariff codes. In this figure, shipment quantities are reported in 1,000 mt and are not converted to dry weight equivalence.

The 1996 levels are close to each other: 157,930 mt for U.S. Customs and 159.77 for SECOFI. The gap widened considerably in 1997: 179,820 mt for U.S. Customs and 338,510 mt for SECOFI. The SECOFI import amount is 88 percent higher than that reported by U.S. Customs. The gap narrowed to about 38 percent in 1998: 207,090 mt reported by U.S. Customs and 285,450 mt reported by SECOFI. Interestingly, the U.S.-sourced numbers show increases in export levels in spite of Mexican compensatory duties for both 1997 and 1998. The Mexican data show a decrease of over 53,000 mt from 1997 to 1998.

Early-Season USDA Projections of Sugar Production

By: Stephen L. Haley 1/

------ 1/ Agricultural economist, Specialty Crops Branch, Market and Trade Economics Division, Economic Research Service. ------

Abstract: This article examines methods used in the early projection period (May-January) by the Interagency Commodity Estimates Committee (ICEC) of the U.S. Department of Agriculture (USDA) for forecasting sugar production. This early period is important because it includes the time when the sugar tariff-rate quota is established and when the first tranche is either allocated or canceled. The quantitatively-based techniques that the Economic Research Service provides as input to the ICEC process are discussed. The article describes estimation techniques for forecasting sugar yield per acre. It also describes the influence of technological improvements on increasing sugar yields and the influence of weather. USDA within-season estimates of sugarcane and sugarbeet yields are analyzed.

Keywords: beet sugar, cane sugar, forecasts, projections, sugar production, sugarcane, sugarbeets.

Early-Season USDA Projections of Sugar Production

Each month, the U.S. Department of Agriculture (USDA) publishes its projections of sugar supply and utilization for the preceding, current, and upcoming (May to September) fiscal years in the World Agricultural Supply and Demand Estimates (WASDE) report. Personnel from several USDA agencies, who constitute the Sugar Interagency Commodity Estimates Committee (ICEC), have the responsibility of making projections. These agencies include the World Agricultural Outlook Board (WAOB), the Foreign Agricultural Service (FAS), the Farm Service Agency (FSA), and the Economic Research Service (ERS). The representative from the WAOB chairs the committee. The projections are closely followed by industry participants (producers and consumers) and by policymakers. The projections are instrumental in determining the volume of tariff-rate quota (TRQ) imports, including the tranches scheduled for January, March, and May.

The first fiscal year (October/September) sugar production, consumption, non-TRQ import, and export forecasts are made 5 months before the start of the fiscal year (FY) in the May WASDE. A complete projection of U.S. sugar supply, utilization, and ending stock levels is made in October after the volume of TRQ imports is established subsequent to the September WASDE. The ICEC meets monthly and updates the projections as new information becomes available.

The periods during which projections are made and revised can be divided into early and later stages. These stages are distinguished by the type of data and **analysis** available on which to make the projections. Prior to the February ICEC meeting, there is not enough Sweetener Market Data (SMD) from FSA to provide an accurate gauge of the current WASDE projections. Up to then, information from a variety of sources, including the National Agricultural Statistics Service (NASS), is carefully analyzed, using statistical techniques and econometric forecasting methodologies in establishing and updating projections. The February SMD report information through December, the end of the fiscal year's first quarter. By then, cane sugar production from Louisiana is largely complete, and enough beet sugar production has taken place to allow for a comparison with what is projected. After February, actual production, consumption, and trade data from SMD play an increasingly important and larger role in revising projections.

The purpose of this article is to examine more closely the methods used in the early projection period, especially August through January, for forecasting sugar production. August is a good starting point for **analysis** because it is the first month that NASS makes yield and production forecasts for sugarbeets and sugarcane.1/

------ 1/ As explained below, projections of sugar yield per acre rely on yield forecasts from NASS. Although sugar projections are made starting in May, it is not until August that actual effects of weather are quantified through yield forecasts in a useful way for making sugar projections. ------

The August-to-January period is important because it includes the

time when the TRQ is established (i.e., immediately after the September WASDE) and when the first tranche is either allocated or canceled. Both have direct implications for the quantity of raw sugar imports available to U.S. refiners. The emphasis is centered on the quantitatively-based techniques that ERS uses as input into the ICEC process. Although actual projections made each month are not necessarily the same as those suggested by the techniques examined herein, the ERS projections focus discussion in the ICEC meeting and help the committee to arrive at a consensus.

Projections for Sugar Production in FY 1999

The ICEC relies heavily on NASS reporting and forecasting during the early part of the sugar production projection cycle. Although NASS does not forecast sugar production, it reports on the production of the primary sugarbeet and sugarcane crops from which the sugar is extracted. The ICEC must join together NASS-generated forecasts of beet and cane production with information about extraction rates. NASS does not report on sucrose content of the primary crops, and is silent on other factors that may influence the sugar extraction rate.

NASS publishes prospective plantings of sugarbeets at the end of March, or about 6 months before the start of the upcoming FY. This and other information, plus an **analysis** of production trends, are major inputs into the initial sugar production projection made in the May WASDE. In June, NASS makes its first acreage harvested forecast for sugarbeets and sugarcane and revises its acreage planted forecast for sugarbeets. It is not until August that NASS makes yield and production forecasts. NASS continues updating and publishing its forecasts of acreage harvested, yield, and production through January for sugarbeets (although there is no report for December) and through March for sugarcane. Revisions are published in June.

Figure A-1 shows WASDE beet sugar production projections for August 1998 through February 1999. Beet sugar was projected at slightly under 4.38 million short tons, raw **value** (STRV), in August. As NASS' forecasts of the size of the beet crop increased, the beet sugar projection was raised, first to 4.42 million STRV in September and then to 4.5 million STRV in November. However, by February, beet sugar production through December from SMD were much lower than anticipated and inconsistent with the 4.5-million STRV projection from January. The projection, therefore, was lowered to 4.4 million STRV. At this point, projecting beet sugar production left the early stage when another set of information (i.e., SMD) became useful.

Figure A-2 shows changes in beet sugar projections and in NASS' forecasts of acreage harvested and yield from August through January. The variables each month are shown as proportions of the corresponding January amount, so all variables converge at the **value** of 1.0 in January. NASS' forecasts of acreage harvested do not change much--less than 1 percent downward over the period. The yield forecast shows greater variation and upward movement, 5 percent from August to January. The beet sugar projection also shows variation and upward movement, but less than the yield. Also, the sugar projection is imperfectly correlated with the yield. The strongest correlated period between sugar production and yield appears between October and November.

Figure A-3 shows WASDE cane sugar production projections through March for each of the cane producing regions, except Puerto Rico, which is not covered by NASS. Hawaiian production is spread out through most of the year. The harvests in Florida and Texas begin later in the fall and can extend into March and beyond. The harvest in Louisiana usually starts in late September/early October and is typically over by the end of December.

Developments late in the season influence NASS forecasts, and thus are not reflected in sugar production projections until later. Also, NASS does not separate out cane for sugar from cane for seed until December. One way is to allocate cane use in the previous year's shares in computing cane for sugar.

Figure A-3 shows a rather flat profile, especially through November.

The largest increases take place in Florida in December and January as the cane harvest gets in full swing. The Louisiana cane sugar projection was increased in December. Compared with Florida, a greater proportion of the Louisiana cane crop had been milled into raw sugar, and therefore, there is less uncertainty regarding the volume of total production.

Figure A-4 shows changes in monthly forecasts of sugarcane acreage harvested, yield, and cane sugar, all relative to the March level (similar to Figure A-2). The profiles are fairly flat through November. Both yield and cane sugar increase from November to December, and all three increase from December to January. (NASS increased its forecast of Louisiana acreage harvested from 385,000 to 400,000 acres.)

ERS Early-Season Projections of Sugar Production

Figure A-5 illustrates the primary method ERS uses to project sugar production during the early season. The method derives from the separation of production into two multiplicative components: acreage harvested and sugar yield per acre. As explained, acreage harvested forecasts are made by NASS and typically do not vary that much during the forecast season.

Sugar yield has several features that can be projected based on available data. The first feature is technical change. Over time, improvements in several areas have been made that consistently and predictably increase the degree of recovered sugar per acre. These areas include milling technology improvements, new mill capacity expansions, harvesting improvements in the field, better disease control, improvements in controlling pests and weeds, etc. Also, for beets, there is the additional recovery of sugar from the desugaring of molasses.

Besides technical changes, sugar per acre is influenced by weather-related events. One way to analyze weather-related effects on sugar yield is to first consider the effect of weather events on primary product yields (cane and beet yields). The effect of weather is typically strong on primary product yields, and the relationship of primary product yields to technical improvements is less certain than it is for sugar yield.

Technically, this means that there is low correlation between technical improvements influencing sugar yields and primary product yields. This low correlation permits interpretation of changes in primary product yields as chiefly related to **random** weather events that change year-to-year. 2/

-------- 2/ Times-series **analysis** reveals that Florida cane yields have been increasing about 0.22 ton a year since 1980 but that only 32 percent of yearly yield variation can be explained by the upward, technically-induced time trend. Louisiana cane yields show no consistent trend from 1980 to 1997, although yields since the mid-1990s have been growing due to the adaption of new enhanced cane varieties. Texas yields show no trend, and Hawaiian yields have been declining, probably due to the retirement of large amounts of productive land from sugar production. Almost all State beet yields show no trend, and there is no trend discernable in aggregate U.S. beet yields. --------

The explicit model representation for sugar yield is:

This equation can be estimated with times-series data to show how sugar yield has been increasing due to technical improvements (coefficient B) and how yearly variations in beet or cane yields have influenced sugar yield (coefficient C). 3/

-------- 3/ Low correlation between primary product yields and time facilitates the interpretation of coefficients "B" and "C". Otherwise, statistical correlation (called multicollinearity) would lessen the reliability of the statistical measures used to measure the significance of the hypothesized relationships embedded in the coefficient values. --------

With estimates for A, B, and C, and with NASS forecasts of beet and cane yields, a projection of sugar yield can be made. This number can in turn be multiplied by the NASS acreage harvested forecast to provide a projection for sugar production.

Lack of available data restrict the level of disaggregation in the **analysis**. There is only a national beet sugar equation because

beet sugar production is reported only on a national level (although NASS forecasts sugarbeet production on a State level). The beet sugar equation can be estimated net of the effect of desugared molasses to isolate on the effect that the other technological factors have on improving beet sugar yield. This estimation can be done because USDA has estimates of the sugar produced from the desugaring of beet molasses. Regional cane sugar equations can be estimated because cane sugar production is reported regionally.

Table A-1 shows regression equation estimation results. The "B" and "C" coefficients are shown, along with standard errors, and computed t-statistics. T-statistic values above 1.96 generally mean that one can reject the hypothesis that the corresponding coefficient is insignificantly different from zero. Also shown is the adjusted r-squared (R2), an indicator of how much of the variation in sugar yield is accounted for by variations in the explanatory trend variable (i.e., technical change) and by beet or cane yields (weather). The closer to 1.0 the R2 is, the better.

Estimation results are generally good. The adjusted R2s are high, especially for the cane equations. The beet sugar adjusted R2s are not quite as high (0.55 to 0.61), partly influenced by aggregation over a wide set of differing producing-area conditions. The "B" coefficients are significantly greater than zero for all equations except Texas and Hawaii. All "C" coefficients are significantly positive, as hypothesized.

The coefficient for beet sugar, net of desugared molasses, is less than half the **value** of the corresponding coefficient in the beet sugar equation. This would seem to indicate that, on average, beet molasses desugaring has accounted for about half of trend growth in beet sugar yield.

The sugar yield equations are used to project sugar per acre. The projection is multiplied by NASS forecasts of acreage harvested to project sugar production for the cane regions and for U.S. beet sugar. The statistical properties of the equations can be used to provide confidence **intervals** (i.e., upper and lower bounds) for the projections.

A qualification to the approach involves the accuracy of within-season yields relative to the final estimates. The final yield estimates are those used in the sugar yield equations, but the within-season forecasts of final yields are used for within-season projections of the sugar yield. First-yield forecasts are made in August, 2 to 4 months prior to the harvest. Each month closer to the harvest provides additional information for making the forecasts more accurate. Given times-series data on forecasted yields and final estimates, it is possible to indirectly quantify how much is learned with the passage of time to the harvest season.

Within-Season USDA Yield Forecasts

The model used to measure pre-harvest yield forecast accuracy is:

Desirable estimation results would be that coefficient "A" is equal to zero, that coefficient "B" is equal to one, and that a very high degree of the variance in the final yield is explained by the estimated equation. Table A-2 shows results for U.S. beet yields, and table A-3 shows results for regional U.S. cane yields. The tables show estimates for coefficients "A" and "B", along with their standard errors and two sets of t-statistics. The first set relates to the hypothesis that "B" is significantly different from zero. A **value** of 1.96 or above is sufficient to conclude that the hypothesis is correct. The second t-statistic relates to the hypothesis that "B" is significantly different from one. A t-statistic less than 1.96 would indicate that this hypothesis cannot be rejected.

The tables also show the adjusted R2 (explained above) and the Schwarz Information Criterion (SIC). The SIC is an estimate of the 1-step ahead out-of-sample prediction error variance. A smaller SIC relative to other SICs within a grouping indicates that the equation is a better predictor of the final yield estimate. It would be expected that the closer-to-harvest yield equation would explain more of the final yield variance (higher adjusted R2) and be a better predictor (lower SIC relative

to earlier month yield forecasts). Month-to-month growth in adjusted R2 and the decline in SIC are rough indicators of how much information is learned between months in successfully forecasting the final yield.

Table A-2 shows results for U.S. beets, aggregated across States and also at individual State levels, from August through November. Aggregate U.S. results are the most useful because the beet sugar equation (table A-1) makes use of only the aggregate U.S. beet estimate. All "B" coefficients are significantly greater than zero, but rise to levels significantly above one. There is consistent growth in adjusted R2s, from 39 percent in August, to 63 percent (September), 71 percent (October), and 93 percent (November). The SICs fall each month closer to harvest. There is an especially large drop going from October to November, as much of the harvest winds down and information about it becomes known and incorporated into the forecast.

Table A-2 also shows results for individual States. Results in six of the 10 States are very similar to the aggregate results. These States include Colorado, Michigan, Minnesota, Montana, Nebraska, and North Dakota. With each passing month the adjusted R2s increase consistently, and there is a relatively large drop in the SIC going from October to November. The "B" coefficients are all significantly greater than zero, and statistically very close to one (unlike the aggregate U.S. result). California results are close to fitting the pattern, but there is not much difference between October and November--practically the same values for adjusted R2s and for the SIC. Hard-to-forecast States include Idaho, Oregon, and Wyoming. Until November, all R2s are low and only rise between 45 to 60 percent by November.

Table A-3 shows results for the U.S. cane regions. Results for mainland producing areas of Florida, Louisiana, and Texas show a pattern of relatively low adjusted R2s until January. The largest decreases in respective SICs take place in January as well. These results indicate that hard-to-predict late-season developments are crucial to cane yield forecasting. Steadier Hawaiian results (i.e., more gradual changes in adjusted R2s and SICs) are reflective of production taking place throughout the year. Thus, late season developments matter less in yield forecasting. The "B" coefficients for Hawaii, Louisiana, and Texas (except August) are all significantly greater than zero. The "B" coefficients for Florida are only significantly greater than zero in September and January.

In conclusion, results indicate that more is known earlier in the season for sugarbeets than for sugarcane, even relative to the respective harvest periods for each. However, once beet or cane production is known with high certainty, implications for cane sugar production seem to be known with greater certainty than for beet sugar production: the test statistics for the cane equations in table A-1 are better than those for beets.4/

------ 4/ Another source of uncertainty for beet sugar production derives from the early-campaign harvesting of the beet crop. If beets are harvested in September and processed that same month, the production gets recorded in the previous year's totals. Crop and fiscal years are now the same and do not begin until October 1. A small amount of Louisiana cane sugar production is typically processed in September as well. ------

An explanation is that cane is processed into raw sugar sooner after harvest than are the beets. Beets are stored in sheds and piles for a longer period during which sucrose deterioration can take place. This is especially true for the Red River producing area, where processing from crops harvested in October can continue on into May and June of the next calendar year.List of Tables Page

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CONTACT: Stephen Haley, Report Coordinator Tel: +1 202 694-5247 Fax: +1 202 694-5884 e-mail: shaley@econ.ag.gov

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By MICHAEL SIMONSEN, PhD BBI Contributing Writer CHICAGO, Illinois - Companies participating in the clinical diagnostics sector are taking different approaches to meeting the changing customer re-quirements wrought by the cost-based turmoil in the health care industry. The bigger players in the in vitro diagnostics field are expanding products and tech-nologies in order to offer as broad a line as possible, while small- and mid-sized companies are focusing their product development efforts on those niches offering opportunities for above-average growth. Some of the latter include: * Nucleic acid diagnostics, with anticipated growth rates of more than 20% a year over the next more than 20% a year over the next several years. * Whole-blood glucose mon-itoring, expected to grow at 10% to 15% a year. * Various immunochemistry market sectors, including car-diac markers, tumor markers, bone disease markers and infec-tious disease tests. * Point-of-care tests for criti-cal blood parameters. * Tests for use in the home health setting. Testing is rapidly moving out of the traditional hospital setting into clinics, outpatient facilities, and into the patient's home. And testing is rapidly moving away from use of broad panels toward disease-focused testing, nudged along by new regulations requiring that approach. So the volume for classical routine chemistry tests is dropping, while demand for spe-cialized tests that directly impact therapy and triage decisions is rising. The pace of new product introduction in clinical diagnostics is probably most rapid in the point-of-care (POC) sector. At this year's American Association for Clinical Chemistry (AACC; Washington) meeting, held here in August, Biosite Diagnostics (San Diego, Califor-nia) exhibited its new Triage meter providing the capability to perform a cardiac panel including CK-MB, myoglobin, and Troponin I in 15 minutes. This product joins the Stratus CS from Dade Behring (Deerfield, Illinois), which offers the same menu and a turnaround time of as little as 13 minutes for one test and 20 minutes for a three-test panel. The Stratus CS does not perform all three tests using a single device, but rather performs one test per single-use

Schiapparelli Biosystems (Fairfield, New Jersey) is another company addressing the non-hospital-based POC testing market, and is about to launch a new test system for chemistry **analysis**.

Schiapparel-li's target market is the physician's office lab. Schiap-parelli has introduced the NExCT system, a smaller **random** access benchtop centrifugal analyzer with closed tube sampling targeted at low volume physi-cian's office labs performing three to five test panels per day. The NExCT is priced at under $40,000, and cost per test for reagents is under 40 cents per test. Schiapparelli estimates there are about 6,000 addi-tional labs that are performing between 5,000 and 25,000 tests per year in the U.S. that are potential placement sites for the NExCT. Many of these sites now have Gemstar analyzers, DT60 systems from Ortho Clinical Diagnostics (Raritan, New Jersey), or Reflotron instruments from Roche Diagnostics (Basel, Switzerland) in place, and probably will be seeking a replacement system within the next two to three years. Schiapparelli expects the NExCT sites to perform about 10,000 tests per year on average, ver-sus an average of around 60,000 tests per year for the ACE. Overall, the new products that are being intro-duced into today's global market reflect the gradual movement of an increasing proportion of testing to sites outside of the traditional hospital and commer-cial reference laboratory, and into sites such as the physician's office, clinics, skilled nursing facilities, and home care. In addition, there is considerable growth in hospital-based point-of-care testing, partic-ularly for tests such as cardiac markers that offer a major potential cost savings if the accuracy of chest pain patient triage can be improved. As a result, the market for POC cardiac marker test systems is attract-ing a number of well-funded competitors, and sales for certain tests such as Troponin I are growing at a 50% to 60% annual rate, according to some esti-mates. Clinical chemistry market trends The market is far from stagnant in many other segments, and new products continue to be launched at a rapid pace in spite of sluggish or flat growth. An example is the serum chem-istry segment, which is experiencing declining sales in some regions, primarily due to reduced test volumes resulting from restrictions on panel testing. Table 2 presents data from the Part B Medicare reimbursement (BESS) data-base showing the trend over the past five years for unit volumes of routine chemistry panel tests submitted to the Health Care **Financing** Administration (HCFA; Baltimore, Maryland) for reimbursement. The data indicate a quite rapid decline in 1996 and 1997 in the total num- ber of chemistry panels of all types following steady growth in volume in prior years. As shown in the table, the decline primarily has been the result of a precipitous drop in Chem 19 panels, whereas the number of Chem 7 panels has continued to increase at a quite rapid rate, exhibiting in excess of 8% growth in 1997. However, the drop in routine chem-istry testing does not necessarily imply that all labs will need smaller, lower throughput analyzers since in many cases labs are consolidating, driving up test volume requirements in the remaining sites even though overall volume is down. And labs that are experiencing a drop in chemistry test demand have needs for new systems that provide workstation con-solidation in order to reduce labor costs to compen-sate for the loss in test revenues. There is significant demand for consolidated workstations that combine various test disciplines in either a single platform or in an interconnected plat-form. For example, Beckman Coulter (Fullerton, Cal-ifornia) exhibited the LXNet at AACC, comprised of a Synchron ALX chemistry analyzer linked to an Access immunochemistry system via a central data station, allowing all test orders and reports to be handled at one console. Anew Power Processor also was demon-strated that auto sorts individual specimen tubes into racks that can then be distributed more efficiently to various workstations. Another configuration is the Chem Xpress, which consists of a sample processing front end plus an LX20 clinical chemistry system. Samples are automatically sorted based on their bar code label, and those destined for the chemistry ana-lyzer are automatically loaded on the LX20 for analy-sis while specimens to be tested on other systems are moved to an output station where they can be taken to other types of analyzers. Roche Diagnostics demonstrated its new Modu-lar sample processor, a system composed of various modules that perform cen-trifugation, decapping, ali-quoting,

recapping, and aliquot sorting, which can be connected via an output buffer to a track system that can convey samples to vari-ous analyzers. Roche also introduced the new Integra 400, a smaller version of the popular Integra 700, as well as new cardiac marker assays for the Elecsys system includ-ing a nine minute Troponin T assay and a CK-MB test. Myoglobin will be added in the third quarter of this year. Roche also demonstrated an automated sorter that allows samples to be directed to either its Hitachi chemistry systems or the Sysmex hematology analyzers, build-ing build-ing on its alliance with TOA Medical/Sysmex (Long Grove, Illinois) to offer combined chemistry/hematol-ogy products to the lab. Olympus America (Melville, New York) is one of the smaller players in clinical chemistry, but the company has continued to invest in new products for this segment and more recently has succeeded with immunochemistry systems and systems for routine typing and infectious agent screening of donated blood. Olympus is promoting standardiza-tion of reagents and test procedures across its prod-uct lines, responding to the desire of many, if not all, lab managers for standardized systems that simplify the management of diagnostic testing in the hospital and lower costs by reducing training and mainte-nance expense, and allow consumables to be pur-chased in higher volumes, thereby increasing the lab's purchasing power. Standardization also is important to most integrated health care networks, since it can allow a patient to be tested at any site within the network and obtain consistent results. A key feature of the Olympus analyzers is their high throughput and short time to result. This feature is attractive to the increasing number of labs that are switching to an "all stat" operating mode, wherein all specimens are run as soon as they arrive in the lab. The Olympus chemistry systems are capable of running a Chem 7 stat profile in under five minutes (to first result), with subsequent results available at 45-second **intervals.** Olympus launched the AU400 Chemistry-Immuno Analyzer at AACC. It provides a test throughput of up to 800 tests per hour and offers a menu of 115 tests including general chemistries, ISEs, special chemistry, and Syva

immunoassays for drugs of abuse, therapeutic drugs, and thyroid markers. Growth in the low-volume, POC sector of the chemistry market may be stimulated as a result of the new partnership announced by Abbott Diagnostics and i-STAT. The partnership involves an equity investment by Abbott of $22.7 million, and calls for Abbott to assume sales and marketing responsibility for i-STAT's products, and to also collaborate in the development of cardiac marker tests for the i-STAT analyzer drawing on Abbott's expertise in immun-odiagnostics. The alliance will build on Abbott's strong existing position in point-of-care testing with its MediSense division. The entry of Abbott in this market segment is likely to drive further expansion of the POC testing market in the hospital. Renewed interest in cellular **analysis** Cellular **analysis** has a wide range of applications in clinical diagnostics, from conventional hematology counts to flow cytometric determination of cell sur-face markers and, most recently, in situ hybridization **analysis** of cellular nucleic acids. While the hematol-ogy sector of the market is one of the primary market segments of in vitro diagnostics, totaling about $1.3 billion worldwide in 1997 as shown in Table 3, this segment is mature, with the limited growth that does exist being attributable to a trend for labs to replace some labor intensive procedures with automation. The flow cytometry segment of the market, totaling about $674 million worldwide as shown in Table 3, continues to exhibit some growth as new applications are introduced, driving an expansion in the consum-ables market. However, as the growth in incidence of AIDS in the developed countries has slowed, the rate of increase in the market for CD4 counts performed via flow cytometry has dropped, and this application has been an important driver of the market over the past few years. Other segments of the cellular **analysis** market have **historically** represented small niche opportuni-ties, even though test volumes can be quite high in the histopathology segment and in PAP smear **analysis.** Procedures have remained highly labor-intensive for the most part in these segments,

with consumables cost staying very low at a few cents per test for con-ventional histopathology slide-staining tests. Automation products for the cellular **analysis** market have not been widely adopted because of their added cost and lack of a clear demonstration of benefit to the patient. Recently, some new companies have developed cellular **analysis** products that may meet with increased receptivity in the market. Two companies with advanced cellular **analysis** systems include Intelligent Medical Imaging (IMI; Palm Beach Gar-dens, Florida) and Chroma Vision Medical Systems (San Juan Capistrano, California). IMI exhibited the Micro21 automated microscope at AACC, a comput-er- based video microscopy system employing a Sony color camera, an automated slide stage, and dual 200 MHz Pentium processors. A white blood cell differential assay is FDA-cleared and available for sale, and the company also markets the Mini-Prep hematology slide maker with a throughput of 120 slides per hour. Several other applications are all also FDA-cleared, but are in various stages of prod-uct launch. A urine sediment test for the Micro21 is awaiting FDA approval. The Micro21 analyzer has a list price of $175,000 ($195,000 including the slide maker), and consumables cost for the slides is about 20 cents each. Chroma Vision Medical Systems is a unit of Excel Vision, a firm founded to commercialize imag-ing technology developed as part of the Strategic Defense Initiative. Chroma Vision is focusing ini-tially on applications in cancer diagnosis and moni-toring, but long-term, the company's Automated Cellular **Analysis** System (ACIS) can serve as a plat-form for a number of cell-based diagnostic applica-tions, targeting automation of the approximately 1 billion microscopic procedures performed today in the U.S. Automated cellular **analysis** has gained increased market acceptance as a result of the devel-opment of systems for performing automated Pap smear **analysis**, including the AutoPap analyzer from NeoPath (Redmond, Washington), the PapNet from Neuromedical Systems (Suffern, New York), the Screen system from AutoCyte (Burlington, North Carolina) - a spin-off of Roche Diagnostics - and the TracCell 2000 from AccuMed International (Chicago, Illinois). The AutoPap has achieved the highest market penetration so far, primarily because the system has received FDA approval for use as a primary screening tool vs. a secondary screening device used to verify slides that have already been screened by a cytotechnologist. The AccuMed sys-tem is also intended for use as a primary screening device. While the automated Pap smear screening sys-tems are dedicated to a single application, imaging technology can potentially be applied to a wide range of tests in oncology, infectious disease, and prenatal screening. Improved cell **analysis** methods could replace existing high-cost surgical procedures for detecting the presence of metastatic cancer cells, for example, with improved sensitivity as compared to existing techniques and at lower cost. Other segments of the cellular **analysis** market, including the hematology and flow cytometry seg-ments, are also witnessing significant new product development activity. Bayer Diagnostics (Tarrytown, New York) has recently introduced the Advia 120 sys-tem, a multi-function cellular **analysis** system provid-ing standard hematology counts plus reticulocyte counts, with a throughput for routine CBC/ differen-tial counts of up to 120 samples per hour. The Advia 120, with a list price of $189,000, incorporates the abil-ity to use either capped or uncapped tubes, continu-ous sample loading, and a pre-treatment module to automate labor-intensive up-front steps in the analyt-ical procedure. While Bayer and the other major players in cell **analysis** - including Beckman Coulter, Sysmex, Abbott Diagnostics and Becton Dickinson (Franklin Lakes, New Jersey) - provide strong competition in the mature hematology/flow cytometry market, at least one additional supplier continues to see opportunities for growth in this sector. ABX Hematology (Garden Grove, Califor-nia), a subsidiary of ABX Hematologie (Montpelli-er, France), introduced four new products at AACC, including a low-cost (under $30,000) hema-tology analyzer with a five-part differential; a reticulocyte analyzer with a built-in slide prepara-tion

module; Hematovision 3 blood cytology soft-ware; and the Micro 60, a low volume (60 test per hour) hematology system also sold by Bayer as the Advia 60. The ABX products were previously dis-tributed by Roche, but this relationship was dis-solved. ABX has placements in approximately 800 labs in the U.S., with a product line including the Argos, Helio, Minos, and Micros analyzers. By 2002, ABX aims at obtaining a 12% share of the hematol-ogy market worldwide in order to move into the No. 3 market share position. The company's worldwide sales at present are about $70 million, with $6 million in the U.S. market.

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Summary

Richard Leftwich, Steven Kaplan
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VAR (**value** at risk) measures the maximum loss that a **portfolio** is likely to sustain over a particular period, given specific assumptions about the behaviour of security prices.

It was developed as an alternative to relying on position limits for monitoring and controlling risks associated with positions held by traders and trading desks. VAR is now applied widely in **financial** institutions for risk assessment, risk-based capital controls and riskadjusted performance measurement.

Although it is superior to the previous generation of risk-management tools, it is far from a panacea even for those applications. Serious conceptual and implementation difficulties must be resolved before VAR can be applied other than perfunctorily.

In addition, it relies on information about trades supposedly provided by an organisation's control systems. But recent **financial** scandals suggest that control systems are the weakest link in the

risk-management process.

The disciples (and the vendors) of VAR are advocating its use in risk-management systems for industrial corporations involved in hedging. Such applications are likely to produce risk measures that are simply inappropriate for corporate risk management.

VAR is not the first **portfolio** management tool to be applied out of context in the corporate arena. Diversification was, and is, an eminently sensible strategy for individual investors. But as a corporate strategy, diversification generally does not add **value** for stockholders.

Risk and **portfolio** managers

VAR measures the exposure of a **portfolio** to changes in market prices under a specific set of assumptions. For example, suppose that a **portfolio** manager holds a $100m domestic government bond **portfolio**. If the rate of return on that **portfolio** is normally distributed with a daily standard deviation of 1 percent, the loss experienced on any one day will exceed $1,6m five days out of every 100 days, so the VAR is $1,6m.

VAR is not a unique number. The probability level and time **interval** (95 percent and one day in this case) must be selected and assumptions made about the statistical properties of the rate of return on the underlying **portfolio** (a normal distribution with a daily standard deviation of 1 percent in this case).

Figure 1 lists VAR estimates for alternative probability levels and volatility assumptions for a normal distribution.

The choice of the time horizon and the probability level are a function of the organisation's ability and willingness to bear risk. For example, choosing a short time horizon, such as a day, implies that early warning signals are important. Choosing a high probability, say 99 percent, implies that losses greater than the VAR can be tolerated only infrequently.

In the simple illustration given below, the **portfolio** consisted of only one security, domestic government bonds. Typical portfolios consist of more than one security or asset class. Moreover, when monitoring trading operations, the positions of different traders or trading desks must be aggregated.

The **portfolio** volatility or the volatility of the aggregate trading position is not simply the sum of the volatilities of the component parts - interdependencies (as manifested by correlations) must also be accounted for.

Proper risk-management techniques recognise that some interdependencies can be risk reducing (as is the case with diversification). By taking advantage of diversification, the exposure of a **portfolio** of a particular size can be reduced or the size of a **portfolio** with a given exposure can be increased. Thus, correlations (or the lack thereof) between and within asset classes are important components of VAR, but these correlations considerably increase statistical estimation problems.

For example, if there are five components (asset classes or trading positions), there are 10 pairwise correlations to estimate, if there are 10 components, there are 45 pairwise correlations to estimate. In general, if there are N components there are N(N-1)/2 separate pairwise correlations.

Determining the appropriate statistical assumptions for modelling the volatility of the **portfolio** is the subject of much research and innovation. Estimation methods fall between two extremes - either the underlying statistical distribution can be represented by a theoretical distribution (typically a normal or lognormal distribution) or a distribution (called the empirical distribution) can be constructed from **historical** data.

Neither method is superior (in theory or in practice) and each has its advocates. Once a statistical distribution - theoretical or empirical - has been selected, probabilities can be associated with potential outcomes.

If an empirical distribution approach is employed, the probabilities of occurrences of given magnitudes are estimated directly from that distribution using Monte Carlo **analysis** or bootstrapping. (These are methods of testing a model using data simulated according to various assumptions, typically relying heavily on **randomly** generated data, or on **random** selections from **historical** data.)

On the other hand, if rates of return are assumed to follow a normal distribution, 99 percent of outcomes are less than 2,33 units of standard deviation from the mean. If the mean is close to zero and the standard deviation is 2 percent per day, this implies that there is only a 1 percent chance that the **portfolio** will decline by more than 4,66 percent on any day (or $4,66m if the **portfolio** has a market **value** of $100m).

By varying the parameters, risk preferences or constraints can be accommodated. For example, for a normal distribution, 90 percent of the observations are less than 1,28 units of standard deviation from the mean, so if the mean is close to zero and the standard deviation is 2 percent per day, there is a 10 per cent chance that the **portfolio** will decline by more than 2,56 percent on any day, or $2,56m if the bond **portfolio** has a market **value** of $100m.

Even in this, its most elementary form, VAR has severe limitations, resulting from: extreme observations, non-stationarity, illiquidity, non-linearities and model risk.

Extreme observations occur because many securities experience a higher frequency of extreme outcomes than is predicted by the commonly employed normal distribution, resulting in a VAR estimate that understates the risk of large losses. Some securities, particularly those with embedded options, have very low probabilities of extremely large losses. Those losses are difficult to capture with theoretical statistical distributions and require a long history to reveal a single bad outcome.

Non-stationarity is a statistical warning that the past is not necessarily a guide to the future. **Historical** data yield poor predictions about future outcomes if the process generating rates of returns changes due to alterations in the underlying economic situation. Under extreme economic conditions, such as the Gulf War or a currency crisis, **historical** relationships, especially correlations, may fall apart.

If securities do not trade in highly liquid markets, reliable prices are not available to calculate rates of return. More critically, if there are large adverse price moves, **portfolio** managers may not be able to sell large quantities of the security without further depressing the price, particularly if other **portfolio** managers are doing the same. VAR will underestimate the severity of bad outcomes unless markets are highly liquid.

Some classes of securities, such as exotic asset-backed securities, either trade in illiquid markets or are so new that an adequate **historical** record of prices does not exist. For these securities, VAR calculations rely on prices derived from models of the relationship between the security and a more fundamental economic variable such as the interest rate.

Actual losses may then exceed the theoretical VAR maximum if the model is imprecise, thus introducing another source of risk dubbed "model risk" or "mark-to-model" risk.

Standard VAR calculations do not allow for non-linear relationships; but, for some portfolios, particularly those with embedded options, non-linear relationships are the norm. For example, a 2 percent change in the price of a security may cause a **portfolio** to lose $1m but a 4 per cent change may cause it to lose $10m. Non-linearities can be accommodated but only at the expense of additional estimation problems, typically due to model risk.

Despite these limitations, VAR is a useful risk-management tool for **portfolio** managers and trading desks. Instead of setting

position limits for traders to limit the firm's exposure to unacceptably large losses, VAR allows each trader's exposure to losses to be restricted directly. Moreover, individual exposures can be aggregated to accurately reflect the exposure of a company by taking correlations into account.

VAR is seldom used in isolation and its efficacy should not be judged on a stand-alone basis. For example, VAR is often accompanied by stress testing or scenario **analysis**, techniques with their own strengths and weaknesses. Even the process of collecting the requisite data for VAR calculations improves risk control in most organisations.

A final VAR caveat. Unless the internal control system records a firm's positions accurately, VAR is akin to whistling in the dark. Debacles such as Barings, Daiwa and Sumitomo provide politically expedient rallying calls for better risk-management techniques. The use of VAR by those firms, however, would not have deprived us of the fascination associated with those catastrophic losses, because the "rogue" traders allegedly did not disclose their positions to their employers.

Risk management for corporations

The stereotypical wheat farmer plays a prominent role in hedging examples used in **finance** textbooks and in marketing material distributed by futures and options exchanges. Rather than bear the price risk associated with this year's crop, risk-averse farmers rationally enter into forward or futures contracts to lock in a price and reduce the variability of the proceeds from the crop sale.

The relevance of those examples for managing risk in a large publicly traded company is dubious. Public corporations are themselves risk-sharing vehicles; and it is difficult to see how risk reduction by the corporation adds **value** if stockholders can reduce risks on their own account at low cost by, for example, diversifying their investments.

Investing in futures and options contracts is, at best, a zero-sum game unless a company's managers have superior information. And managers with superior information should be trading on that information (pejoratively called speculating), not hedging.

VAR applications in corporate risk management have two drawbacks: VAR does not measure the exposure that is relevant to **value** -maximising corporate risk managers; and VAR is misleading in the presence of illiquid assets on corporate balance sheets, especially if accounting rules do not reflect economic reality.

It is accepted that, in the classic Miller-Modigliani model of the firm, risk management per se does not add **value** to the firm. Departures from that model reveal that risk management can, under certain conditions, increase the company's cash flows. Those conditions involve the presence of either: progressive corporate tax rates, high expected costs of **financial** distress or short-term **financing** constraints. Some would add investor clienteles and management performance systems as additional possibilities.

Although these conditions justify corporate risk management they do not justify VAR as a risk-management tool. VAR is based on the assumption that the volatility of changes in **value** is of paramount concern. The volatility of changes in **value** (of the firm or of the equity) is almost irrelevant in an economically justifiable corporate hedging policy.

Consider first how risk management can add **value** by smoothing taxable income when tax rates are progressive. Suppose that the first $5m of profits are taxed at 20 percent and profits above that level are taxed at 40 percent.

If a company reports taxable profits of $1m one year and $7m the next year, its tax bill will be $2m on profits of $8m. If adroit use of futures contracts allows managers to smooth taxable income so that $4m is reported each year, the total tax bill for the two years will be reduced to $1,6m.

Similar effects can be demonstrated if tax losses can be carried forward but not backward to earn a refund. Managers who engage in derivatives transactions to reduce income taxes follow strategies to lessen

the volatility of reported taxable income and are not concerned about the volatility of changes in the **value** of the company or of the equity. VAR is uninformative about their strategy.

Alternatively, suppose that the corporate risk management programme is designed to reduce the expected cost of **financial** distress, which depends on the probability of **financial** distress and the costs of **financial** distress if it occurs.

Financial distress reduces a company's cash flows if suppliers, employees and customers are not willing to trade with it on the same terms if distress is likely. Apple Computer provides a classic example of distress costs now that its existence is in doubt. Customers are reluctant to buy a durable good, software developers are skittish about investing in products that are specific to Macintosh computers and employees are reluctant to invest in firm-specific skills.

If there were **financial** instruments with payoffs negatively correlated with Apple's fortunes, Apple's stockholders would benefit from lower costs of **financial** distress if management hedged using those instruments. Unfortunately, other than the stock of Intel and Microsoft, those instruments are not traded and it is difficult for a corporation to sell its own stock short.

Some short-term **financing** constraints create a role for risk management but, again, VAR has little relevance here, because profit-maximising managers should focus on reducing the mismatch between cash required for short-term investments and cash available from **financing**, especially from internal **financing**. In contrast, for companies with ready access to capital markets (such as those with highly rated debt), it is difficult to see how risk management (particularly interest rate risk management) adds **value** for stockholders.

The intuition behind risk management for financially constrained business is as follows: if cash available from internal and other **financing** sources falls short of cash required for potentially profitable investment projects in some states (for example, when oil prices are high), managers can reduce or eliminate the costs of forgoing those projects by investing in **financial** contracts (for example oil futures) that pay off when the undesirable states occur.

Financial constraints are necessary but not sufficient to create **value**-maximising demand for hedging of this kind. It must also be the case that, in bad times, a company's investment demands do not decline by as much as its available cash flows decline.

For example, consider two firms who face short-term **financing** constraints and whose fortunes depend heavily on the price of oil: an integrated exploration and production company and a natural resource group that pursues growth by acquisition.

The oil producer's cash flows decline if the price of oil falls but its demand for investments in new oil exploration projects declines also since, at low oil prices, oil exploration is not as profitable. Hedging contracts that pay off if the price of oil falls will not add **value** since they will produce cash flows when investment demand declines.

On the other hand, the natural resource company believes that, when times are bad, acquisitions are more profitable because companies can be bought at "fire sale" prices. Such a company might add **value** by hedging to ensure that, in otherwise bad times, it has adequate funds to acquire distressed properties. When times are good, the hedging activities will restrict the availability of funds but lucrative acquisitions are then scarce.

A "pure play" argument in favour of hedging is sometimes given. It is argued that some stockholders would prefer to invest in a company's main line of business but avoid some of the ancillary price risks associated with some inputs or outputs.

For example, a "pure play" airline would allow investors to take only

the risk of airline operating and marketing efficiencies by hedging oil price (fuel) risk.

Even if there were such a class of investors, hedging to accommodate them would increase firm **value** only if the company could extract a premium from those investors. The logical and empirical validity of that possibility has not been demonstrated.

Finally, some theories of compensating management suggest that better performance measures could be obtained if the effects of some price changes were removed from measured performance. Why that purging should be achieved with hedging instead of through the accounting system has not been demonstrated.

Of course, there may be managerial incentives to hedge if the ownership of the corporation represents a considerable part of management's wealth and if the corporate control system allows managers to focus on maximising their utility rather than on maximising the **value** of the stock. Hedging by these companies does not add **value** to stockholders, but VAR does not measure the costs imposed on stockholders by the unnecessary hedging behaviour.

Even if the VAR concept corresponds with a company's hedging objectives in a corporate setting, VAR provides little relevant information because, for most non-**financial** companies, many assets and liabilities are not liquid and accounting rules do not mark even all liquid assets to market.

Consequently, VAR tells investors about the exposure of its **financial** instruments to gain or loss but not about potential gains or losses for the remainder of the firm's assets and liabilities. Nevertheless, in 1995, the US Securities and Exchange Commission adopted VAR as an acceptable method of providing required information about a company's derivatives activity. Why information about a subset of a firm's assets (derivatives) warrants such attention reflects politics, not economics.

These limitations of VAR are mitigated for companies with highly liquid assets and liabilities, such as banks and insurance companies. They are close analogs of the trading companies and portfolios that were the origins of VAR and it is rational for them to reduce the volatility of their capital (assets less liabilities) so that the same capital can support a larger investment base or so that a given size of operations can be **financed** with less capital.

However, even for **financial** institutions, the presence of illiquid assets or liabilities on balance sheets and accounting rules that do not mark even all liquid assets to market distort incentives if VAR becomes the focus of regulators.

Regulators of banks and **financial** institutions have embraced VAR as a regulatory tool. The Basel Committee of the Bank of International Settlements has proposed that the capital requirement for commercial banks be based on VAR. VAR is defined as the maximum loss that will be incurred over a 10-day period with a 99 percent probability and capital is then set at three times that VAR.

Others who have followed suit in adopting VAR for capital adequacy standards, albeit with different parameters, include: the European Union Capital Adequacy Directive, the International Swaps and Derivatives Association, the Group of Thirty, the Derivatives Product Group and, in the US, the National Association of Insurance Commissioners.

Conclusions

Like all tools, VAR has its limitations and it offers naive users false comfort. Nevertheless, it belongs in the risk-management arsenal for monitoring and controlling the risk of trading positions and investment portfolios.

Using VAR in a corporate setting is another matter entirely, especially for industrial corporations. They may have legitimate reasons to manage some of the risk they face but VAR is not likely to be an informative indicator of the efficacy of those risk-management programmes.

VAR fails in a corporate setting because, for most non-**financial** companies, many of the assets and liabilities are not liquid. Consequently, VAR tells investors about the exposure of the **financial** instruments to gain or loss, but not about the gains or losses for the remainder of the company's assets and liabilities (such as a gold mine's reserves) or about the relationship between gains and losses on the hedging instruments and gains and losses on its other assets and liabilities.

Richard Lefwich is Fuju Bank and Heller Professor of Accounting and **Finance** at the University of Chicago Graduate School of Business. His research interests include audit qualifications, bond ratings, corporate charter changes and block trades.

Steven N Kaplan is professor of **finance** at University of Chicago Graduate School of Business. His research interests include mergers and acquisiitons, corporate governance and private equity.

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A friend called us up and asked what was going on in the logic IC markets. Specifically, our friend asked, what packages are going to be used and how many pins will these packages have.?

Packages

Our predictions probably reflect a more optimistic expectation of the migration toward more sophisticated packages and higher lead count devices. We feel this rate of migration is justified by the demand that is going to be put on electronic products to be smaller and more powerful. To become smaller and more powerful, electronic product design is at the place where it has to push upstream, toward the IC itself. The IC package is the printed circuit board of the future. These "systems" on a chip will then be tired to other systems for greater integration. Now where there is a modem board, soon there will just be a modem chip, a memory chip, a logic chips, all encased in one package.

The biggest lesson that has been learned by the development of the computer market is that smaller is better. When the computer is small enough to be easily shoved to a remote part of the room, people want them.

If prices could be reduced, the notebook market would explode--a half dozen to a household in a years time.

Another need, like smaller size, that will drive the IC market toward higher pincount devices is going to be flexibility. Electronics needs to learn to mold itself to the world. The huge base of consumer appliance products will be tapped, in part, by better product flexibility, and greater flexibility will be achieved by the use of fewer, high pincount devices, because the overall mass of the product is reduced by reduced package designs.

A packaging consideration that is going to drive the move toward higher pincount devices is the development of array packages, especially ball grid arrays (BGAs). Quad flat packs (QFPs) have reached upper limits in pincount because of material considerations in lead construction. With leads the size of spider's silk, proper placement was tremendously daunting. Tape automated bonding (TAB) was supposed to help this situation, but, because of the equipment cost, probably. TAB had a hard time catching on, although there is a good deal of renewed interest in TAB and some promising products But BGA has all the inherent stability of pin grid array (PGA) packages, with none of the PGAs disadvantages, which were many, not the least of which was PGAs ate up a lot of board real estate.

System on a Chip (SOC)

Despite the rapid advent of systems-on-silicon, experts say the industry is immature, groping for tools to tackle business and legal challenges. While technical hurdles such as verification and test need solutions, it's the business-model issues that are commanding the most attention. Today's cores come with a confusing array of licensing and pricing options, raise legal issues, such as patent indemnification, and lack adequate protection against software piracy. Moreover, the nascent third party IP business faces a potential collapse through a quick devaluation of cores, some observers said. That could happen if silicon manufacturers give free access to cores.

"The IP business model isn't working," said Gary Smith, an analyst at Dataquest Inc. (San Jose, Calif.), as he introduced an IP98 panel. "There's nothing wrong with the business; we just have to find a model that works.

Andy Graham, president of the Silicon Integration Initiative (SI2; Austin, Texas), commented at another panel that there is no viable IP "infra structure." What's needed, he said, are standards, licensing conventions, legal protection, vendor qualification, customer support and a marketing channel.

The role of EDA and ASIC vendors is muddled and is growing combative. Cadence Design Systems (San Jose) took some heat for its move into chip-integration services at one panel, where John Danne, executive vice president at LSI Logic (Milpitas, Calif.), warned that EDA companies should not become ASIC vendors.

Despite the obstacles, no one at the conference disputed the compelling need for commercial IP. A new market forecast from HTE Research (San Francisco) estimated that the IP market is growing at an annual rate of 100 percent and will reach $1.4 billion by 1999.

Perhaps the biggest potential challenge to IP providers is a rapid decline in prices. The drop may have already begun: Smith told of a USB core that initially fetched $250,000 in royalties but was down to a $20,000 initial purchase with no royalties within a year.

"The effect of devaluation on the IP market should not be underestimated," said Philippe Delforge, head of IP business operations for Alcatel Microelectronics. "There is a risk that the IP market will collapse because large silicon manufacturers start to give free access to their IP with the sole purpose of winning the silicon bidding war."

Delforge said the industry is divided into two strata: high-**value**, low-volume IP, such as that in leading-edge cores, and low-**value**, high- volume IP, found in "commodity" cores. It's the latter category that is at risk if silicon manufacturers choose to lower non-recurring engineering (NRE) costs by giving away intellectual property.

The consensus that's emerging is that there will be a variety of licensing models. "A single method of IP delivery does not suit everyone," said Doug Ridge, business-development executive at Integrated Silicon Systems Ltd. (Belfast, Northern Ireland).

System on a Chip

Imagine buying a system-on-a-chip--even processor core-based silicon--for less than $20. Cirrus Logic's (Fremont, CA) 208-pin VQFP-packaged chip with its $18 price tag offers a lot of bang for the buck, and is a good example of a system-on-a-chip approach.

At the same time, another silicon vendor is dishing up a heavily integrated system-on-a-chip product--also in a 208pin VFP. That firm is Taiwan-based Integrated Technology Express, and its product is a $20 peripheral controller oriented for Windows CE HPCs, portable DVD players, and the like. This device should sidestep dedicated ASICs and real-estate consuming multichip designs. Significantly, it packs an interface that directly handshakes with Hitachi's increasingly popular SH-3 Series 32-bit RISCs.

Dubbed the IT8101, ITE's chip works in lockstep with Win CE. Its power management unit lets Win CE monitor the chip's internal functions, including its VGA LCD controller, infrared circuits, a 2-slot, multivoltage PCMCIA interface, UART and RS232 interfaces, interrupt controller, and timers. If any of these blocks are inactive beyond a programmable **interval**, they're shut down. When peripheral activity resumes, the PMU handshakes with Win CE to rum blocks back on. External functions are also throttled through the IT8101's GPIO port.

The IT8101's LCD controller supports 640 x 240 pixel screens, and--in light of Windows CE v2.0--can generate from 256 colors to as many as 64,000 colors or 64 gray scales. The controller also manages up to 512 kbytes of external video RAM.

With its genesis in the Cirms Logic CL-PS-7010 as designed for the Newton MessagePad 2000, Cirrus's latest edition builds on the ARM-based CL-PS7110, which is currently clocking away in the belly of Psion's Series 5 PDA. As it steps into the PDA and smartcellphone limelight, this latest CLPS7111 iteration, with an ARM710A core at its heart, adds several enhancements to its predecessor's already extensive power-management suites, It averages 66 mW of dissipation while running at 18 MHz (at 3.3 V). Packed with scads of peripherals and power-management hooks, it should readily support handhelds powered by a couple of AA or AAA cells. It will idle at 15 mW and draw 15 microAngstroms with its realtime clock running but everything else stopped. For a two-cell system, it'll also operate at 2.7 V.

Mixed-signal ASICs becomes "System-on-a-Chip."

Mixed-signal IC technologies allow design engineers to reduce complex, multiple IC designs to a single system-on-a-chip (SOC). Such highly integrated, monolithic devices are less costly, consume less power, and have a much smaller footprint than implementations based on discrete ICs.

The latest motor-control chips are typical of this trend toward integrated single-chip mixed-signal systems. Until recently, three-phase motor-control systems were designed using several analog and digital discrete ICs to implement the various functions of the signal chain. Motor control system design engineers require increased complexity in the techniques used to implement advanced sensorless control schemes while reducing system costs. These requirements have created a demand for embedded DSP-based, mixed-signal motor control SOC from semiconductor companies. This situation makes great demands on the technical understanding of mixed-signal designers and requires careful choice of design methodologies and tools.

Mixed-signal and analog design

Many companies are faced with the problem of how to put high-speed analog on the same chip with digital circuitry. The basic problem is that the digital circuitry produces a great deal of noise that can affect the

analog circuitry. Currents flow in the substrate of the chip and interact with other elements, causing, offset voltages and noise in the system.

Along with the noise from the digital side, the outside environment can be very noisy due to high-frequency signals, voltage spikes, EMI and EMC that must be filtered out. Typically, most of the inputs are differential to help eliminate much of the noise from the outside world. Instead of having an input reference to ground where any noise on that one line gets amplified, a differential input is used to cancel out the input noise.

Successfully putting digital and analog circuits on the same substrate requires isolation of the digital from the analog side of the chip. Several kinds of isolation are required to deal with power rail noise and chip bounce. Power rails have to be separated and multipath grounding has to be provided. Designers have to understand where ground loop and surge currents now. They have to understand something about the accidental coupling of parasitic capacitance. When transistors run at a high speed in small geometry processes, they inject charge into the substrate, which is a minority carrier that may end up in some part of the analog converter where it can create problems.

With sigma-delta and pipeline hash converters, it helps to put the signal on chip as a differential signal. That way, with a careful job of balancing all the loads and displacement currents getting on and off chip, any balanced noise like chip bounce that hits both sides equally is a common mode noise. Consequently, rejection of that spurious signal depends on good common mode rejection.

Using differential inputs cuts down on noise pickup, particularly through power rail bounce. The end user, however, is looking at three different windings with three different signals in the motor and these aren't differential signals. At some point, you have to decide where to turn a single-ended signal into a differential signal.

For analog design and simulation, Analog Devices (Wilmington, MA) uses a proprietary internal design tool. Modeling isn't just done at the transistor level. It also includes modeling of ah the substrate effects, pads, and packages, letting you characterize the design in a real world sense. You must understand the loading effects of the bond pads and other structures, as well as the consequences of packaging. Differential input won't help if these loading effects aren't considered.

One of the design's most critical aspects is the clock signal, since the system can't tolerate clock jitter. You need to under stand what kind of noise couples into the clock signals, and which power rails will have current spikes that could cause a shift in the clock. If, for example, a system is running a buffer on the clock line going to the ADC, and it isn't a low impedance line, it could cause considerable clock jitter. Static timing **analysis** (provided in the Synopsys toolset) is used to find such problems.

From a digital standpoint, the design process is fairly generic, although there are unique requirements for interfacing to the analog elements and embedding the DSP. To the extent possible, industry standard tools are used to execute the digital design now.

Motor-control digital designers use Synopsys (Mountain View, CA) Design Compiler for design synthesis. Verilog code development and circuit synthesis are used in this environment to develop the circuit. Engineers also use a code coverage tool (VeriSure from Cadene Design Systems--San Jose, CA) to hell evaluate the statements of the generated Verilog code. This tool helps ensure that the code has been checked and exercised in simulation.

Schematic design is often accomplished with Cadence Composer, which allows manual design entry and helps to cohesively integrate the analog design portion with the digital design. Engineers netlist out of that environment for the final physical and logical verification. Layout vs. schematic verification validates a physical layout against the transistor level netlist, while logical verification is completed using Cadence's

Verilog XL and Synopsys' timing **analysis**. Analog Devices six output lines--which drive the power amplifier--will interact. The PWM circuits must have tight control of the edges and timing of the pulses in the output.

New Frontier helps design systems-on-a-chip

We' re not sure we're quite prepared to invest our own money in a company like this, but this is the sort of innovation that we feel is going to open up the market for very high-level, silicon-integrated products.

Belgian EDA firm Frontier Design has opened a stateside ASIC design center here to implement what it calls "algorithm-to-silicon" designs. Targeting systems-on-a-chip, Frontier's design center will focus on performance-differentiated DSP for telecom and multimedia applications, using off-the-shelf devices. Reusable intellectual property cores for wireless telecom and consumer audio will be bolstered by a toolkit that includes a Mentor Graphics Mistral synthesis system.

Innovative Processes bring systems on chips to life

True cell-based system-on-chip (SOC) technology involves more than just placing huge amounts of digital logic on silicon. To implement fill electronic systems on chips, you also have to be able to design or place other types of blocks--precision analog, special memories, and, for some designs, RF--on that silicon. Good EDA tools and design methodologies are necessary for successful SOCs. However, the essence of true SOC design is silicon processing that supports multiple design technologies on a single chip.

The processing technologies you need to design technology blocks on silicon require process foundries to modify high-speed digital-logic processes. These modifications-often, add-on process modules--increase the cost of the baseline digital process. Along with adding silicon cost, this approach may lower performance for modules, such as analog blocks, designed with the added processing than you can get with a separate chip fabricated in a process optimized for that block type. However, the cost, power, and speed advantages of SOC designs often outweigh alternative multichip-based systems with individual chips optimized for digital, analog, and memory functions.

Most ASIC companies approach SOC process support with modular processing. The companies start with a high-speed digital-CMOS process and add process masking and other steps to implement technologies on the digital process. These technologies include precision analog; high-density SRAM, DRAM, and flash memory; and BiCMOS for RF or high-current-drive applications. Of these technologies, analog is the most important add-on for SOC-based systems. Unfortunately, adding analog capability to a digital CMOS also creates process- and circuit-design problems.

A merged-logic/DRAM process requires around 35% more process steps and is one-third more expensive than the baseline logic process. You can get as much as 128 Mbits of DRAM on a chip with I/Os, or words (in ASIC terminology), as wide as 1024 bits. But a process like Samsung's flash-memory technology is only available for Samsung's 0.35-micron process now, although the company says it's migrating the process to a 0.25 micron process. Analog core designs need one or two additional masking steps-one for metal-to-metal capacitors and a second for poly-to-poly capacitors. Adding bipolar transistors to create a BiCMOS process for RF cores requires four more masks. The BiCMOS process lets you design I/Os with speeds as high as 2.4 GHz.

SOC Components

You can't build all the systems you need on your chip. You buy many and make your money arranging and utilizing them profitably. Artisan seems to want to help this market develop. Most ASIC libraries include some SRAM capability, either with fixed blocks or by using an SRAM compiler. ASIC companies either internally develop the technology or get it from the a third-party embedded memory vendor through a purchase or a technology agreement. But Artisan, an embedded SRAM vendor, offers process specific memories tuned to a customer's process that represent the high end of

third-party embedded SRAMs.

Something DRAMatic for Developers

Although some semiconductor companies combine DRAM processing with digital processes, start-up Silicon Access recently announced DRAMatic, a one transistor, high-density embedded DRAM core. DRAMatic cores come in a range of word widths and depths. The high-I/O-bit cores are interesting for SOC applications because they provide higher memory-access speed because they don't have to go off chip to interface with logic. Single-chip logic and DRAM also result in lower power dissipation than having the two functions on separate chips. Common logic and DRAM eliminate many of the pins needed for off-chip DRAM support. The resultant SOC's reduced pin count can substantially lower chip-package cost.

You can use DRAMatic for a merged DRAM/logic chip either by adding processing steps to a foundry's logic process or by using a DRAM process and adding metal layers to support digital logic. Most SOC designs strive for maximum logic speed, so you may end up using the high-speed logic process with added DRAM processing because the baseline DRAM process reduces logic performance. 7 he additional processing for DRAMatic adds approximately 10 mask layers and costs about 20 to 40%, more than digital-logic-only processing at 0.25 micron. Silicon Access offers DRAMatic as a core for a targeted application or as a DRAM compiler. Core prices are approximately $100,000 to $150,000; the company has not yet set compiler prices.

If programmable-logic vendors can overcome the technical challenges of placing analog or mixed-signal cores on FPGAs, the demand for such devices will probably remain low. On processes with similar dimensions, programmable chips are slower than cell-based chips. Because of this performance gap, cell-based designs remain the implementation vehicle for your SOCs for the foreseeable future.

Can SOC designs be FPGA-based?

Leading-edge programmable-logic chips can contain hundreds of thousands of logic gates, so you might wonder whether any FPGA- or CPLD-based SOC designs exist? The answer is "no" if your definition of an SOC chip is one with large amounts of digital l(logic, analog cores, and different memory blocks. Many of the leading programmable-logic companies, including Actel, Altera, and Xilinx, have aggressive programs with third-party core providers for both soft and hard cores on FPGAs or CPLDs. However, these programs now include only digital cores.

Quad Announces Sale of SMTech to Speedline Technologies and OEM Agreement to Market and Support Stencil Printer Product Line

We found this interesting. Quad benefited greatly by the development, in the U.S., of the market for mid-level placement equipment. As with many company once they'd made some money, they seemed a little uncertain about what to do with it. The ended up buying SMTech, a British stencil printer company. But their attempt to expand that business in the U.S. was met with some of the toughest competition imaginable, and, perhaps, they just didn't know the stencil printing business as well as they did the component placement business. (Management at SMTech in the U.S. was taken on by people who had been at Quad.)

For whatever reason, Quad announced the sale of its SMTech printer business to Speedline Technologies, Inc., a subsidiary of Cookson Group. Under the agreement, Speedline's MPM Division will supply Quad on an OEM basis with the former SMTech stencil printer product line. Quad continues to offer SMT manufacturers fully integrated QuadLine production solutions.

"This agreement allows Quad to continue strengthening its core SMT and selected APT (advanced packaging technology) assembly businesses while at the same time enhancing the printer offerings we provide to current Quad customers and the industry as a whole," said Ted Shoneck, president of Quad.

"Quad and Speedline/MPM have combined their technology and manufacturing resources to deliver market leading stencil printing solutions," said Craig Ramsey, vice president of marketing for Quad.

"Quad's advanced products and systems integration expertise are strengthened by MPM's stencil printing market knowledge and experience. Quad will continue to offer best of breed assembly solutions to SMT manufacturers world wide."

Bob Balog, general manager of Speedline/MPM, commented, "With the joining of SMTech and Speedline/MPM's product lines, the electronics assembly market has access to the full range of stencil printer products, from benchtop semi-automatic units to the most advanced automatic printers in the world. We look forward to expanding our product line by adding SMTech's cost-effective and flexible printers."

Darpa Looks to Optical Interconnects

The Defense Advanced Research Projects agency is mapping out an aggressive program to develop optical interconnects at the board and hip level in a bid to save billions of dollars in defense-electronics spending. The plan was outlined by Anis Husain, assistant director of the agency's electronics Technology Office. Husain described the current status of Darpa-funded optical interconnect Projects and presented a plan for the future. One factor that will have a profound effect on the implementation of board-level optical interconnects is the sudden commercial emergence of the verticalavity surface-emitting laser (VCSEL). Husain asserted that the "vertical-cavity laser is to photonics as CMOS is to electronics."

Fueling the excitement surrounding VCSELs is their recent achievement of striking performance gains and size reductions. Early lateral-emitting diode lasers had an awkward, 5-micron x 1,000 micron geometry; the latest VCSELs have a round aperture. In addition, the diodes radiate light vertically, making them convenient for packaging in array configurations.

"These VCSEL breakthroughs will be a key enabler for VLSI photonics," Husain said. The current research goal is to push the diodes to 4 square microns and develop packaging and mounting techniques to integrate them with CMOS VLSI chips, he said.

Another significant breakthrough is the advent of high performance plastic fiber. Graded-index fibers made from per-fluorinated polymers have realized a 200-times improvement in bandwidth loss over previous plastic-fiber technology and could cut interconnect costs by a factor of 10, Husain said. The high-efficiency Fiber, coupled with efficient VCSELs, could reduce the power cost of interconnect at the backplane from 100 mW to around 1 mW.

Characterizing the previous long-haul fiber-optic generation as one in which "spectral density" dominated, Husain said subsequent generations will, like silicon electronics, be characterized by increasing "spatial density" as optical technology moves from board to interchip and on-chip connectivity.

A New Balancing Act tan Advanced SMT Assembly?

The concept of balanced one off surface mount technology assembly line using precision placement systems and solder paste dispensing yields a relatively high volume production capacity that is fully software programmable, even to the point of being able to handle one board at a time assembly! The only major limitation is the low number of different components that the pick-and place machine can load at a time.

Two very different technology developments make this concept a reality today. **Historically**, both precision component placement machines and adhesive/solder paste dispensing equipment were too slow for even moderate to high volume assembly. For any real production volumes, stencil printing of solder paste and a combination of high speed chip shooters with Precision component placers for fine-pitch components were, and still are, used by both captive and contract SMT assemblers.

What is changing this picture! First, extensive miniaturization of components as well as products dramatically increasing component density on most products, particularly in portable products such as cell phones. The advent of 0402 and even 0201 passive components, use of low profile fine-pitch quad flat packages (QFP) and rapid deployment of chip scale packages (CSP) increases the proportion of parts on any assembly demanding

precision placement capability. Second, over the past 10 years the sophistication and cost of image processing necessary for high speed, precision placement has advanced tremendously, along with the speed and versatility of dispensing system a

A quick review of component placement fundamentals is in order. Several years ago Don Spigarelli of Sierra Research & Technology described component placement to me in terms of ballistic, tracer and guidance targeting. A ballistic targeting machine has a fixed machine origin from which all coordinates and adjustments are calculated. The machine must be provided with a component map defining the fixed coordinates at which each component is to be placed. The boards and components are then presented to the placement machine as accurately as possible. Very simple vision systems at the component pickup point may be used to facilitate component adjustments for rotation and translation errors from their presentation to the placement machine. Ballistic systems are the fastest component placement machines, but they must be built with great precision and repeatability. Ballistic systems are also susceptible to lead screw wear, as well as variations in printed wiring board (PWB) geometry resulting from multiple supplier s or even simple process variations, as in the PWB singulation process. Finally, all error is accumulated from the corner of the PWB that is closest to the machine's fixed origin.

More advanced component placement systems, described as tracer and guidance systems, employ more sophisticated vision systems and algorithms to find and fix the origin of the PWB placement map. In tracer targeting, the vision system observes specific fiducial marks on the PWB and calculates the location of the component placement map origin for each PWB as it enters the placement operation. This eliminates the need for great precision in the machine manufacture since the origin for all component placements is observed and adjusted for each PWB separately. These machines still demand excellent repeatability, but are not as susceptible to lead screw wear. Any dimensional variation errors are accommodated from the center of the PWB, which eliminates the effect of board to board edge variations and reduces the impact of dimensional variations in component lead pitch or PWB pad location. However, these errors are still accommodated from the corner of the component, which accumulates all error at the furthest corne r from the PWB origin.

Guidance targeting uses more sophisticated vision methods to find the placement origin for each individual component on each PWB. This eliminates even the need for built-in repeatability since the machine actually "looks" at the component and the intended location to find the best fit between the two before actually placing the component. For large, tine-pitch components this method accommodates all error from the center of the component, thereby reducing the accumulation of error at the corners of the component through averaging.

The more complicated image processing requirements of tracer and guidance technologies make these machines slower than ballistic systems. However, they are far simpler to set up and maintain, and they are well suited to mixed product loading and small lot manufacturing. For hue-pitch leaded devices ((less than)0.4 mm pitch) a ballistic machine generally may not be capable of sufficient accurate component placement for high assembly yields, particularly for peripherally leaded devices that do not take advantage of the selfalignment characteristics of area array packaging technologies. For this reason guidance and, more frequently, tracer targeting based component placement dominate hue-pitch and high density assembly.

In the past, ballistic placement could provide placement rates up to 12,000 components/hr or more, while tracer and guidance placement could only achieve rates of 1,500 to 2,000 components/hr. The primary limitation was the slow image processing capability of earlier PC based systems. Conversely, expensive computer imaging systems provided greater speed, but were much more expensive. Today, tracer targeting takes advantage of

specialized image processing hardware, as well as greatly improved software algorithms, to achieve placement rates approaching 7,500 components/hr.

In the near future, the introduction of wide angle imaging and simultaneous, multiple component image processing will bring even greater speeds, along with the addition of guidance targeting capability. The sophisticated vision systems that are being developed can even read the part number off of the PWB and pick the correct component map from memory for "on the fly" product shifts in the production line!

Next issue, we'll look at trade-offs between solder paste dispensing, stencil printing and equipment line balancing made possible using this new approach.

Probing Fine-Pitch ICs

Market research indicates that engineers are often frustrated with current probing technology, specifically the problem of attaching probes to fine-pitch circuitry. A probe is the essential conduit between an oscilloscope or logic analyzer and the device under test. In an ideal world, a probe would connect easily to any integrated circuit, have little or no inductance or capacitance, offer infinitely high resistance, and come bundled with a range of accessories. Unfortunately, today's probes do not meet these requirements, and the challenges have been complicated by semiconductor advances such as increasing bus widths, faster clock speeds and diminishing IC package size.

Solving the Connection Problem As chip designers pack more functionality into ICs, spacings, sometimes as tight as 0.65 or 0.5 mm, make it difficult to hold a probe in place. And if the IC's probe pin requires grounding, a third hand is needed to operate the oscilloscope or logic analyzer. Many engineers work around this problem by soldering wires on an IC's pins. But this can introduce other problems -- from issues of heat to the difficulty of removing soldered wires before the product is shipped. Still others use fine-pitch IC clips, which require shutting the board off and introducing other problems in the troubleshooting process.

A special adapter now addresses these key sources of frustration by providing a way to probe three or eight signals on 0.5 and 0.65 mm IC packages. The adapter features compressible "conductors" that are inserted into the spaces between the IC pins and connected to pins on the opposite end of the adapter. The compressible conductors hold the probe in place, permitting the checker to work hands-free. In addition, each conductor makes physical contact with one side of the pin, creating a redundant physical connection with two contact points that increase the reliability of the electrical connection. In effect, the adapter provides accurate, mechanically noninvasive contact with IC fine-pitch pins with little chance of shorting adjacent pins or damaging the device.

Package Inspection

Inspection to find these anomalies is needed as part of process monitoring and control, as well as for final product quality assurance. Acoustic Micro Imaging (AMI) is widely used to inspect and analyze packages because, by using ultra high frequency ultrasound, it makes hidden internal anomalies visible.

AMI is frequently used for process monitoring, control and final product quality assurance. Within these broad parameters AMI plays many roles, including straightforward failure **analysis** of relatively small numbers of parts; automated screening of large numbers of packages in JEDEC trays; and the automated evaluation of board-mounted components. Although it is most commonly used to image and analyze air gap type defects, it is also widely used in the characterization of device and packaging materials such as molding compound uniformity.

Acoustic microscopes use high frequency ultrasound (5 to 500 MHz) to image the internal features of samples. There are basically two types of instruments:

* the C-mode Scanning Acoustic Microscope (C-SAM)
* the Scanning Laser Acoustic Microscope (SLAM).

The SLAM operates in a through transmission mode and is the fastest

instrument for image production. The C-SAM operates in the transmission mode and the reflection mode. Because the C-SAM has more functions available, it is the type of instrument described in this article.

Ultrasound is sensitive to variations in the elastic properties of materials and is also sensitive to locating air gaps (delaminations, cracks and voids). The sensitivity to thin laminar flaws is unique to ultrasound and is probably the most common reason for its use to inspect samples such as integrated circuits, ceramic capacitors, flip chips and MCMs.

U.K. startup to license optical-IC technology

Bookham Technology Ltd., a U.K. chip startup, plans to license its pioneering active-silicon-optical-circuit (ASOC) technology, with which it makes optical ICs in standard silicon processes on silicon-on-insulator (SOI) wafers. The decision comes as Bookham nears the completion of its $10 million production facility, which it calls the first wafer fab built specifically to make optical circuits in silicon.

"We are actively pursuing a licensing strategy and would expect to have something on an individual product basis within 12 months, said Andrew Kickman, chief executive officer anti president of Bookham Technology. Rickman said Bookham intends to use its fab for R&D and for small- to medium-volume production of standard and custom circuits. Bookham hopes to sign licensees that would build larger production lines to make optical circuits in high volume. "It's really a question of how we best deploy capital to build something of the ASOC technology, said Rickman.

Bookham's fab began making optical transceivers as standard products for fiber-to-the-curb and fiber-to-the-home applications a couple of months aqo, although wafers are still sent to the nearby Rutherford Appleton Laboratory(RAL) for some work. Bookham used RAL's facilities to develop its ASOC process. But it ramps its own wafer fab,

Bookham has added staff and now employs about 150 workers, with about 70 assigned to the fab. Rickman declined to disclose optical transceiver sales by the company, which is privately held. As a follow-up to the transceivers, Bookham is developing integrated optical circuits for dense wavelength division multiplexing (DWDM) applications for 1999.

The company has heretofore discussed the licensing of its ASOC technology in only general terms, but that strategy has now moved onto a fast track. Rickman said the first licensees could come from the Far East, where Bookham obtains laser diodes. "We have some potential outsources and we're talking to them," Rickman said. "There are companies which want to make our chips under their own badge, and there is the possibility of reciprocal trading with piecepart suppliers." Laser-diode maker Rohm Corp. is one potential licensee.

To make its optical transceivers, Bookham mounts diodes on a silicon substrate and aligns them with waveguides defined in silicon on top of a buried oxide layer of the SOI wafers. While Bookham's fab will be capable of manufacturing about 500,000 devices a year, Rickman said the market will require millions of optical ICs per annum within two or three years.

The fab's modest $10 million price tag is due to the fact that it does not use advanced silicon-processing techniques, wafer sizes or machinery. The fab uses standard 2.0-micron silicon-processing equipment and 4-inch wafers, although the equipment is scalable to 6-inch wafers.

Bookham can not make light emitting or light-detecting devices in silicon, nor does it provide amplification. As a result, a large part of its design work is focused on micromachining silicon to simplify its use as a substrate to carry compound semiconductor optoelectronic devices and to provide links between them.

TAB

People with an investment or interest in tape automated bonding (TAB) continue to promise the automated IC delivery system a great deal. One of the key features is the ability to do failure **analysis** in the tape delivery system. "Testing on the fly" describes their vision. This seems like a story we've run every year for the past six years, but a "process" has been developed and tested by Chip Supply (Orlando, FL), with

help from the Center for Microelectronics Research (CMR) at the University of South Florida, called "SofTAB." With SofTAB, known good die (KDG) are attached to conventional TAB bonds, with gold bumps on the die. This allows test and burn-in using conventional TAB sockets. Since it uses conventional single-point bonding, it permits removal of the leads using a proprietary tool, causing damage to neither the die or its bond pads.

Two of the main problems with KGD, production delay and cost, are being addressed by this process. Special handling of bare die delays the release of KGD with respect to their packaged product counterparts, and that special handling costs more to perform. SofTAB, like the DieMate system from Texas Instruments (Dallas, Texas), puts the die in a more robust carrier that can be probed using conventional techniques. The ultimate goal is to release KGD and their packaged counterparts at the same time, with reasonable price parity.

Atmel, AMD proclaim BGA flash standard.

Moving the adoption of chip-scale packages (CSPs) closer to general use by portable-systems developers, a packaging standard covering pinout and footprint specs for high-density ball-grid-array (BGA) flash has been adopted by Advanced Micro Devices (AMD) and Atmel. The standard has also been proposed to the Joint Electronic Devices Engineering Council (JEDEC) Committee. In terms of realworld products, the standard applies to AMD's fine-pitch BGA for flash ranging in density from 4 Mbits to 64 Mbits. Atmel's package is a 6 x 8 array with a ball pitch of 0.8 mm.

National Rolls Smallest Footprint Op Amp

National Semiconductor has developed a new wafer level package for dual CMOS op amps encased in a chip-scale packaging process claimed to leave the final product about the same size as the die itself. Additional products are expected to appear later in National's new Micro-SMD package. National's LMC6035IBP is a general purpose dual op amp optimized for low power applications, measuring 1.45 mm square, in a leadless MicroSMD package applied to the die entirely at the wafer level using a patented encapsulation process on the front and back of the wafer. Standardized JEDEC "bump" pads with 0.5mm pitch assure circuit board placement accuracy using existing passive component assembly chip shooter mounting equipment. The device's 0.90mm height easily meets the requirements of all PCMCIA and other height-sensitive applications. National is looking to license the Micro-SMD packaging technology to others, but no deals have yet been reached. In addition to op amps, other IC categories expected to follow in National's Micro-SMD package include regulators, timers, A/D converters, temperature sensors and comparators.

Fujitsu Trims Relay Package by 25%

Fujitsu Takamisawa America Inc. has unveiled a four-pole signal relay that provides the same functionality as a pair of two-pole relays, but occupies 22% less circuit-board space. The volume relay is also 25% smaller in costs about 40% less, according to the company The FTR-B2 relay series was developed for line-card switching (applications that have required three relays in the past). With the trend toward reduced equipment size, however, now only one four pole or a pair of two-pole relays are needed. OEM pricing for the FTR-B2 relay is $2.70 in 10,000-piece quantities.

BGA Socket Reduces Deformation

A new, patented surface-mount BGA socket from Aries Electronics Inc. (Frenchtown. N.J.), can help to reduce solder ball deformation, according to the company. Aries BallLock BGA sockets we're designed to prevent solder balls from becoming deformed because of the softness of the material from which they are made.

GaAs at Fujitsu

We sang the praises of GaAs many years ago, before the U.S. telecommunications deregulation. At the time the materials and processes were new and expensive, while the applications were virtually non-existent outside the military. But volume production has slowly picked up. As the wireless communications industry expands, and we feel the wireless communications market is going to expand very quickly during the next five

years, demand will increase rapidly.

In 1991, Japan's Fujitsu Ltd. began making products in what was once considered by some to be the "Spruce Goose" of the semiconductor industry. Fujitsu's folly turned out to be the world's largest and most expensive gallium arsenide fab, a $500 million 4-in-wafer plant that was intended to make highspeed parts for the company's own supercomputer lines, as well as for competitive systems from now defunct Convex, Cray Computer, and others.

But when the supercomputer market collapsed in the early- to mid 1990s, Fujitsu was saddled with a ton of GaAs capacity and basically one customer-itself The company had to overhaul its worldwide GaAs operations last year, forming a new subsidiary, Fujitsu Quantum Devices Ltd., based in the Yamanashi prefecture in Japan.

Today, having been forced to stand on its own feet--while shouldering burden of profit-and-loss responsibilities-Fujitsu Quantum hopes to make a name for itself in what's becoming a hot market for GaAs devices, especially the communications business.

In doing so, Fujitsu Quantum's relatively new U.S. subsidiary, Fujitsu Compound Semiconductor Inc., San Jose, is quietly beefing up its sales and marketing operations, expanding its product **portfolio**, opening design centers, and moving into the distribution channel.

More important, Fujitsu is shifting its GaAs-device operation from a mere captive supplier of components for its own telecommunications products, to visions into a major commercial supplier.

"It looks like Fujitsu is making a strong push in the merchant market," said Kenneth Taylor, who follows the GaAs business: for Kenneth Taylor & Associates Inc., a Los Altos, Calif.-based consulting firm.

And Fujitsu could surprise a few people in the process-namely the traditional GaAs suppliers like Anadigics, NEC, Oki, TriQuint, Siemens, and Vitesse.

"Fujitsu Compound looks like they have a very promising story, but Vitesse, TriQuint, Anadigics, and other GaAs-device suppliers have been involved in the merchant market for a much longer period," Taylor said.

Billed as the technology to replace silicon back in the 1980s, GaAs turned out to be too expensive and exotic to use in most mainstream applications, and was pushed out by tradition al parts based on CMOS and BiCMOS technology. GaAs suppliers then focused on the military market.

In the past two years, however, technology developments and highvolume production capabilities have helped reduce production costs considerably, drawing the attention of OEMs throughout the communications industry.

"This has helped increase the usage of GaAs devices in several mainstream applications." Taylor said. For example, the percentage of GaAs devices is increasing in handsets. And in many cases, GaAs is replacing bipolar devices, Taylor added.

Solder Bump Flip Chip

Twenty years after its invention, the use of solder bump flip chip assembly was restricted to a few high volume, deep pockets manufacturers. IBM developed solder bump flip chips in the mid-1960s for their mainframe computers. Since the 1980s, Delco has put tens of millions of flip chip automotive electronic modules under the hood. Solder bump flip chip gradually became the technology of choice for other high volume applications, such as electronic watches, but it remained out of reach for lower volume manufacturers because of the technical complexity and high capital investment required for solder bumping wafers.

However, in the past five years, three developments have made the flip chip advantages of small size and high performance widely available. Solder bumping is now offered as a commercial service, meaning users can purchase bumped semiconductor wafers instead of doing the work themselves. In addition, a variety of less complex flip chip technologies have been developed that have notable advantages over solder bumps in some applications.' One of these, adhesive flip chip, allows bumping and flipping individual chips that can be purchased as die, eliminating the

need for complete wafers as starting material.

Adhesive flip chip is the most promising of the new technologies, and there is a growing body of data about its characteristics, reliability and benefits. Adhesive flip chip advantages over solder bumps include:

* closer spacing
* simpler, lead-free processing at lower temperatures
* flipping single chips.

Adhesive flip chip can connect to standard bond pads spaced on 150 micron centers, or even smaller pads at closer spacings, without the additional "redistribution layer" required for solder bumping closely spaced contacts. Typical adhesive curing temperatures of 150°C are well below those of lead-based solder.

A major advantage of adhesive flip chip over wafer-based processes is that it allows flipping single chips -- bumping and connecting individual die, rather than wafers. The solder bumping process requires entire semiconductor wafers as starting material, producing thousands of bumped chips per wafer. This suits solder bumping well for the high volume production applications it was developed to serve, but can be expensive and inefficient for product development, prototype and production startup. These preliminary stages typically require relatively small quantities of many different chips, instead of thousands of the same type. Single chip flipping solves this getting started problem. Flipping individual die of only the types and quantities needed avoids the time, expense and waste of bumped wafers. Wafer bumping can be postponed until the product is developed, tested and ready for high volume production.

The single chip flipping process described uses gold stud bumps and conductive adhesive for making flip chip connections to off-the-shelf integrated circuit (IC) chips. The process was developed with a variety of test devices and IC chips ranging from simple logic circuits to large **random** access memory (RAM). More than 1,000 assemblies totaling over 15,000 interconnections have been completed during process development, with consistent results and acceptable yields.

General Approach

Single chip flipping combines two well known packaging processes, wire bonding and adhesive die mounting, but reverses the usual order. Chips are used as purchased, without reducing their thickness, remetallizing the bond pads or adding a redistribution layer. Pads may be smaller and more closely spaced than the common dimensions. Any chip that can be wire bonded can be bumped and flipped. The chips, in a temporary carrier, have a gold stud bump formed on each bond pad by a wire bonder. The bumped die are removed from the temporary carrier and mounted on the substrate or board with conductive adhesive. After the conductive adhesive is cured, the assembly can be electrically tested and reworked to replace defective die or poor connections. Easy rework, if needed, eliminates the known good die (KGD) problems of bumped wafers. Finally, the tested assemblies are underfilled with a nonconductive adhesive to seal the space between the die and the substrate, for ruggedness and environmental protection.

Stud Bumping

The gold stud bump is one specific solution for the problem common to all flip chip processes: how to penetrate the insulating aluminum oxide coating of the bond pads and make a permanent connection to the underlying metal. Thermosonic wire bonders, which apply heat, pressure and acoustic energy to make the connection, have been used for many years in gold wire "ball" bonding. For flip chip stud bumping, the wire bonder software is modified so that after forming the ball and attaching it to the bond pad (the first steps in making a wire bond), the wire is deliberately broken off above the ball. The gold ball, or "stud:" that remains provides a permanent, reliable connection through the aluminum oxide to the underlying metal. In addition to the electrical connection, the stud is a mechanical spacer, to keep the die surface away from the substrate, and to provide some relief for the mechanical stresses of thermal expansion and contraction.

Adhesive Application

Conductive adhesive is applied by directly dipping the stud bumps into a thin layer of adhesive or by stenciling adhesive onto the substrate bond pads. To focus on the assembly process, rather than on the characteristics of various materials, the adhesive and underfill materials, applications and curing are standardized. The conductive adhesive is Poly-Solder and the underfill is EL- 18.

Dipped adhesive application is a two step procedure:

A thin layer of conductive adhesive is spread onto a smooth surface. The spreading is done by "doctor blading" a small amount of adhesive onto a flat surface.

The glass plate with a spread adhesive is placed in a flip chip aligner and the chips are robotically dipped face down into the adhesive.

In the stenciled adhesive process, conductive adhesive is applied in a precision stenciling machine through metal stencils, depending on the bond pad size and pitch.

Substrates

Different substrate materials serviced different purposes in the process development. Resistor grade alumina substrates are primarily for thin film hybrid circuit and microchip module (MCM) assemblies. Glass substrates permit visual inspection of alignment, adhesive and underfill after assembly. Silicon substrates isolate the effects of Z-axis thermal expansion mismatches between bumps and adhesive by minimizing the XY-plane expansion mismatch between the substrate and silicon chips. Organic substrates, such as FR-4, polyamide and flexible polyester, are used for special assembly applications.

Chips Process development required mounting and testing a variety of silicon and ceramic chips including digital and analog ICs, memory chips, patterned test chips and arrays.

Test chips with conductor patterns are used to investigate the mechanical and electrical performance of the conductive adhesive contacts. The ICs are used to verify the functionality and electrical performance of stud bumps placed on standard aluminum IC bond pads. The RAM chip tested stud bump uniformity at a higher pad count, and the array tested dipped adhesive uniformity over a larger area. In total, process development required flipping more than 1,000 standard IC chips and test devices, making more than 15,000 flip chip connections.

Assembly

The assembly process is similar for both stenciled and dipped adhesive assemblies. After adhesive application, the chip and substrate are aligned using an SEC-$ 10 semiautomatic flip chip aligner-bonder. The substrate is placed on the work holder, with the chip held above it in a vacuum collet. Chip and substrate are simultaneously viewed through a split-view television camera. After the operator manually aligns the chip and substrate bond pads, the camera moves aside and the chip is placed onto the substrate. The assembly is removed from the aligner-bonder and the conductive adhesive is oven cured to the manufacturer's data sheet recommendations. The assembly may be sample tested or fully electrically tested after curing, to check both the interconnection integrity and chip performance. Defective chips or

Intel Revenue Up For 3Q, Income Flat

Intel reported record revenue yesterday, evidence of the revitalized PC market. But income remained disappointingly flat.

For its third quarter, ended Sept. 26, Intel had revenue of $6.7 billion, a 9% increase over $6.2 billion for the same period last year, and up 14% from $5.9 billion in the second quarter of this year. Net income for the third quarter, however, was $1.6 billion, basically flat compared with last years third-quarter income but up 33% from $1.2 billion in the second quarter this year.

Intel attributes improvements in this quarter to the fact that the reviving PC market has eased the company's inventory glut. Intel also released products this quarter that cater to specific markets--including

its Pentium II Xeon and Celeron processors--and that helped boost revenue, executives said.

"We've made progress in the third quarter to bring expenses under control and reduce head count," said Andy Bryant, corporate VP and CFO, in a conference call. The company plans to bring the total workforce reduction for the year to 3,000 employees, as previously announced. Looking to next quarter, Intel expects to see a slight revenue increase from the third quarter, leading to overall higher revenue for the second half of the year over the first half. The company expects to see improvement this year over 1997.

Critical Issues in Electronic Packaging Assembly

For any business organization, it is of utmost importance to understand the critical issues facing the industry in which it competes. A classic example of this principle is the railroad companies in the 1920s. These organizations failed to realize that their customers' critical issues were cost, speed and destination. Instead, they viewed the industry too narrowly, focusing only on railroad transportation technology. When air transportation technology brought a revolution in the transportation industry, the railroad magnates did not participate because they had not viewed it as a competing technology. Hence, they missed out on an important opportunity for providing greater speed and new destinations, such as overseas, which were the customers' critical issues. The disastrous consequences for not recognizing the critical issues in the transportation industry are now well known

As electronic packaging assembly organizations look to the next century, we find ourselves in a profitable and exciting industry. In the next few years, with the possible exception of agriculture the electronics industry will be the world's largest--greater even than the automotive industry. Present projections show the electronics industry be $1 trillion with a real growth of 7.5%. When one then consider the 5.2% a year price in electronic products, the actual volume of products is expected to increase by more than 13% per year. Since the electronic packaging and assembly business is driven by electronic product volume, the outlook is very favorable indeed. When one also considers that the electronics revolution is in its infancy similar to the auto industry in 1915, strong growth should continue in directions that we cannot predict today. However, we must also exercise caution since our business has **historically** been cyclical.

Considering this factor, it is important for those of us in the electronic packaging assembly business to recognize the critical issues in our industry and address them in a timely fashion, thereby minimizing the risk of following in the footsteps of the railroad magnates. In light of this need, we have investigated the critical issues facing the electronic packaging assembly business. This task was performed by literature searches, discussions with customers and colleagues, participation in national technology "roadmap" development and working with consultants.

The first critical issue is the explosive growth in the number of passive discrete components or "chips." The use of passives has grown from about 100 billion in 1985 to nearly 700 billion in 1994. The latter figure is more than 10 times the number of people that have ever lived! It is a surprise to many that this trend is occurring since silicon integration was expected to reduce the numbers of passive "chips." We will explain why this trend is happening and what is being done to achieve cost competitive solutions to this unheralded challenge.

Second is the tension between ultrafine-pitch quad flat packs (QFPs) and ball grid array (EGA) packages. Approximately 7 billion plastic OFPs will be placed in 1995, yet ultrafine-pitch (0.3 to 0.4 mm lead spacing) configurations are difficult to assemble. While the BGA is in the middle of a typical seven-year development cycle, it shows much promise. It has a much more robust assembly process Yet on the downside, it is an inherently more and requires special attention to board layout, process control and rework. Reliability questions remain as BGA configurations continue to

evolve. Thus, many design engineers are confused as to which of these packages to use. An **analysis** of this dilemma and expected trends will be discussed.

Another issue identified is implementing direct chip attach (DCA) technology. DCA, also called flip chip, can be considered the ultimate packaging technology. It eliminates the first level of packaging, thus reducing cost and increasing electrical performance. While practiced for years at IBM and Delco, it is just now emerging in the industry in general. Implementing DCA is a formidable task, however, because of the difficult assembly and circuit board-related challenges. We will review, in some detail, this exciting technology and steps that are being taken to improve the yield, cost and reliability of this process and final product. The fourth issue is non-traditional assembly such as electromechanical, mechanical, RF(radio frequency) and opto-electrical Non-traditional assembly will be a greater rage of electronic circuit board assemblr in the future. Some may become industries themselves. We will discuss these trends and industry responses to these assembly technologies.

Finally, the end of paperwork is also a critical issue. Computers are affecting our lives and our business more and more. **Value**, which used to be primarily in traditional material form, is now becoming more and more based literally in ones and zeroes. What effect will this trend have on the electronic packaging assembly business? There are sonic pleasant surprises; the U.S. in general has some advantages over Far East competitors in this arena.

Although we tend to malign the U.S. where it is not competitive, we often overlook where we are strongest. Agriculture is a case in point. We export twice as much corn as the rest of the world combined, and we are the world leader in wheat exports. The U.S. stands alone as the unchallenged producer of food in the world, as well as microprocessors, software and other high-technology products.

It is interesting to note that overall growth is approximately 12% per year for all packages. Many people have that the passive discrete component count should drop as integration increases. The growth in passive use has been about 25% per year or so, until recently, when it has dropped to 15% per year. From about 25% in the mid-1980s to nearing 90% in the rmd-1990s, this trend is one of the most striking in the industry, decreasing. We do not see the size going much below 0402s (40 X 20 mils = 1 X 0.5 mm) because of handling issues.

What is the reason for this trend? This question was asked of Professor Peter Krusius of Cornell University. His **analysis** concluded the following. Passive resistors serve two functions: transmission line termination and current limitation voltage "pull up." Transmission line termination is required to minimize unwanted signal reflections, whereas IC component I/O terminals that are not used in a particular application (open collector outputs) must be "pulled up" to the line voltage to allow the IC to operate properly. This process is accomplished by using resistor discretes between these terminals and the line voltage power supply grid. Capacitors are used to decouple switching noise. This noise occurs on the power supply grid during digital switching. In the extreme case, a one could be misread as a zero and vice versa. To reduce the effects of this noise on performance, capacitors are placed throughout the circuit and charged to the line voltage. When switching causes a perturbation in the line voltage, the capacitors "dump" current into or out of the power grid to maintain power supply stability. This power stability helps ensure signal fidelity.

We have answered why passives are needed, so why are their numbers not increasing? Professor Krusius concluded that there are four "drivers" in increased passive use:

1. increased active component I/O
2. higher clock frequencies
3. lower operating voltages
4. Increasing number of analog applications.

It is interesting to note that all of these "drivers" are the current trends. I/O) on active components is increasing, while clock rates have gone beyond 100 MHz. To conserve power on portable units, operating voltages are going below 3 V, and many new products, for example in communications, incorporate analog functions. Hence, one can expect to see a continued strong use of passive discretes.

This discussion begs a question, however: Why can't more of the passive function be integrated into levels of packaging? There are several reasons. First, the active components, such as a specific microprocessor, are used in many applications. Each application would require its own set of passives. In a sense, the circuit needs to be tuned for each application. It is difficult to perform this tuning at other than the board level. Finally, transmission line terminations and decoupling capacitors need to be located throughout the package for best results.

The increased need for passives has created concerns about the cost of placing them. Currently, a turret style chipshooter can place about 250 chips/sq. ft/hr. in floor.

Plastic quad flat packs (PQFPs) are clearly dominating the market for IC (integrated circuit) packaging, with a total of approximately seven billion used in 1995. At higher lead counts, for instance above 200, lead spacings can go below 0.5 mm to as close as 0.3 mm for some packages with 300 leads. Unfortunately, as spacings become tighter, the yield loss becomes greater, exponentially increasing with the closer lead spacings. Competitive yields for 0.4-mm lead spacings are in the neighborhood of 50 to 100 ppm/lead; hence, a 200-lead QFP has about a 15,000 ppm (1.5%) chance of having one lead failure.

As spacings become closer, the chances of solder bridging increase. With 0.3-mm spacings, even control of the solder paste particle size becomes critical because even a small quantity of small particles, such as (15(tilde), will cause "balling," a common cause of solder bridging. As spacings become smaller, control of lead coplanarity and spacing tolerance are critical and more demanding. It is no small wonder that few companies in the U.S. have implemented 0.4-mm technology and none have gone with 0.3 mm. In Japan, a few companies have had success with 0.3 mm, but they had difficulties maintaining acceptable yields.

On the positive side, QFPs are quite easy to inspect and rework because all of the leads are visible and are accessible to rework. This makes the possible yield "hit" somewhat easier to live with since the defective assembly does not have to typically be discarded.

Multichip modules and TAB address needs for higher circuit densities and performance, coupled with manufacturing and testing improvements, in smaller spaces. These technologies continue innovation brought by standard discrete SMT packages such as the small outline package and associated SMT assembly. Advances in circuit design must include interconnection, assembly, and test, and are forcing a more general. more all-encompassing definition of packaging.

Semiconductor substrate typically makes up only about 5% of the board. The remaining surface area is dedicated to chip interconnection, I/O, and manufacturability and testability features.

The multichip module is a packaging technology which has been driven by performance, board density, and mechanical requirements for assembly and test. A multichip module reduces critical interchip delays and allows greater I/O performance where a discrete functional unit subset of the circuit can be defined.

A further advantage of multichip modules is that since they combine several semiconductor chips in one package, they allow the integration of several chip processing technologies into one circuit package. For example, a circuit might require a digital CMOS gate array in combination with bipolar analog functions. The multichip module is often the most economical and reliable way to accomplish such integration. Military devices use multichip modules for reliability and high performance. The redundant MCM, a military construct, packages for example an extra SRAM on the substrate

which is not used unless the primary SRAM fails. MCMs save size and weight in systems such as missiles and space systems where these parameters are critical.

An assembly technology which contains important advantages for multichip modules is tape automated bonding (TAB). TAB allows the reliable fine-pitch assembly required for high I/O, high frequency, high density multichip modules.

TAB is a fine pitch assembly and packaging technology in which integrated circuits are placed onto a substrate by transfer from the surface of a tape.

The three principal TAB approaches are conventional TAB, pocket TAB, and flip TAB. In conventional TAB, the usual method, the chip leads extend from the top of the IC downward to rest on the substrate. Pocket TAB is a low-profile technology in which the IC rests inside a hole in the substrate. Flip TAB inverts the IC and attaches leads from the inverted bottom of the chip, leaving the IC die more clearly exposed to the heat sink above.

Current TAB production is at the 4 mil pitch level, with 2 mil capability coming soon. The 7 mm to 70 mm wide tape consists of two or three layers of copper, adhesive, or plastic. The tape has a series of holes, or windows; onto each window is attached an IC. The IC surface is "bumped" prior to or after mounting on the tape. The small bumps of solder or adhesive on the IC form the bond with the target substrate. Interconnects extend over the window opening to hold the IC in place and to provide the interconnect array for positioning and mounting.

Precision sprocket holes along the edge of the tape facilitate reel-to-reel operation. One reel spins to take up the tape which unwinds from the other reel. The process begins when the sawed and bumped wafer die are attached to the tape surface by an inner-lead bonding machine. This machine aligns the tape to the die and attaches it by applying pressure, heat, or other bonding methodology. Later, the IC die is mounted onto the target substrate using similar methodologies.

TAB may be used for placing ICs onto board substrates or onto multichip modules.

Technological developments in TAB include tape materials engineering, high lead counts, and new bonding and ILB technologies.

Applications demanding the high performance, I/O benefits of TAB include the U.S. military and telecommunications industry. The Japanese and European consumer electronics industries and the worldwide telecommunications industry require small sizes as well as increased I/O.

Chip on Board (COB) is the Emperor's New Clothes of IC packaging - it's no package at all. The IC die is placed directly onto the board substrate during assembly of the circuit.

COB is a packaging approach used with high density circuits in consumer electronic products such as watches and small calculators. Its use will expand as demand for small systems and highly dense circuits proliferate.

Constraints imposed by the current generation of wire bonding equipment limit COB substrate sizes to about 4" x 4". Improvements in wire bonding technology include new resin materials and application methods.

One impediment to COB has been the reluctance of chip manufacturers to ship ICs out the door without packages. Packages provide isolation and protection for the ICs, and IC manufacturers make money on the packages.

Test and inspection of COB present problems associated with the lack of package leads, the high density of circuits in small COB systems, and the close contact between chip and board. Advances in automatic optical inspection systems are solving some of these problems. Particularly difficult is electrical in-circuit testing, in which comprehensive testing of dual-sided boards with line spacing under 10 mil is required.

In sum, COB is appropriate where the benefits of small size and high density outweigh the considerable technological barriers. In the late 1990s these barriers are likely to be overcome, making TAB the technology of

choice for future electronic systems.

Reliability and solderabity have been problems for some SMT IC components.

The EIA in 1990 addressed the reliability problems associated with surface mount devices (SMDs) through proposed standard EIA 583. This standard relates to the problem of damage caused to SMDs from moisture adsorbed during shipping and storage. Moisture can cause the IC to crack or otherwise deteriorate in integrity or performance. The EIA proposal recommends the use of moisture adsorbing desiccant packets, moisture sensors, and special packing materials.

Wave soldering is the general approach to through-hole soldering. SMT uses either infrared reflow soldering or vapor-phase soldering. Forced convection is a heating technology used in conjuction with infrared reflow soldering which allows precise control over thermal processes. Infrared reflow enjoys more support among process engineers than vapor phase due to these advantages.

The heat management problem poses rigorous challenges to integrated circuit package designers. Smaller, more powerful, denser integrated circuits make the problem a packaging problem as we enter the submicron era in microelectronic.

Cooling may be addressed at the board or system level to some extent, as by a fan blowing air across a populated circuit board. Cray and other supercomputer manufacturers immerse some or all of their circuitry into cool liquid such as liquid nitrogen.

The MCM package allows greater I/O, speeds, complexity, and gate counts, but causes significant thermal management problems.

The small-outline (SO) package has generated the most acceptance among SMT designers through 1991. The J-bend, or SOJ, package has leads which bend down and under the IC, saving precious board space and leading to a sturdy lead connection. The alternative gull-wing SO has leads which extend away from the IC, allowing easier inspection and better thermal dissipation for the packaged unit.

The need for higher pin counts in ICs drives packaging innovation. The DIP package is suitable for pin counts below 70, with most products falling into the 15-45 pin range. The chip carrier package, such as the PLCC, is generally used with pin counts of 50-110. The upper limit for chip carrier is about 150. the PGA spans a pin count range of 60 to over 200.

Lead counts of perhaps 500 are possible with the QFP. TAB and flip chip technologies are at the horizon of I/O expectations in the future, extending the range up to perhaps 750.

IC and system designers are looking to optical interconnection technologies as clock speeds for high end computer systems approach and eventually pass the 100 MHz level. First implemented as high speed interconnect links between mainframe computers, optical interconnects are being applied to meet performance requirements at the board and multichip module level.

The delays associated with electrical transmission between ICs and through IC packages are becoming more significant. Further improvements at the high end will likely require optical solutions such as the computer generated holographic optical element (CGH), a fast glass optical substrate material. Optical technology promises fast, highly complex interconnections for computers, and is likely to become very important in the late 1990s.

Some of the key areas of interest for manufacturers of ICs, packages, systems and subsystems are multichip modules, tape-automated-bonding, chip-on-board, and materials and processes.

MCMs are assemblies of unpackaged semiconductors, must like hybrids and chip-on-board assemblies. Multichip assemblies (MCAs) are one of the two modern branches of the

MCM family and are often described by such names as chip-on-board and TAB-on-board. MCAs are nothing more than fine-pitch SMT assemblies, but they define the next generation of PWBs. Multichip component packages (MCPs) represent the more difficult branch of MCMs. Often consisting of two

to 10 ICs packaged in a single leaded or leadless enclosure. MCPs are usually fabricated by the hybrid manufacturer or the semiconductor industry. Presented as an alternative to ASICs and custom semiconductors, this type of MCM affects the PWB industry much as semiconductors have in the past. That is, the MCP reduces the complexity of a PWB by reducing the total pin count and area required for a specific logic function.

Many future semiconductor systems will integrate several semiconductor chips into one package, allowing the combination of several chip processing technologies into one circuit package. Systems involving digital CMOS, bipolar, linear and optical technologies in one module will require packaging expertise and process investment. For example, a circuit might require a digital CMOS gate array in combination with bipolar linear functions. The multichip module is often the most economical and reliable way to accomplish such integration.

The industry consortium Microelectronics and Computer Technology Corporation (MCC) will be an important vehicle for development of advance multichip module technology. There are not yet any standards for sizes and pinouts, for example, of multichip modules. MCC has generated the Quick Turnaround Interconnect (QTAI) multichip module, which is an attempt to simplify and reduce the cost of MCM development.

QTAI consists of an alumina or silicon substrate, on which copper polyimide layers are added. Standard layout and high performance materials are features of QTAI. The principal advantages of copper polyimide are support of line widths of 1 mil and below and excellent thermal conduction.

An assembly technology which contains important advantages for multichip modules is tape automated bonding (TAB). TAB is 'a good choice for integration of bare IC die into modules. TAB allows the reliable fine-pitch assembly required for high I/O, high frequency, high density multichip modules.

TAB will be required in multichip modules and in a growing number of future electronic systems. TAB is a fine pitch assembly and packaging technology in which integrated circuits are placed onto a substrate by transfer from the surface of a tape. Current TAB production is at the 4 mil pitch level, with 2 mil capability coming soon. TAB may be used for placing ICs onto board substrates or onto multichip modules.

Successful IC market participants will understand and implement as appropriate technological developments in TAB such as tape materials engineering, high lead counts and new bonding and ILB technologies. The U.S. military and the telecommunications industry represent two market segments that demand the high performance and I/O benefits offered by TAB. The Japanese and European consumer electronics industries and the worldwide telecommunications industry require small sizes as well as increased I/O.

The increasing desire for small, powerful products will fuel demand for chip-on-board technology. One of the principle ways of mounting the chip of the substrate is in a "flip-chip" arrangement. Flip chips are unpackaged silicon ICs whose bonding pads accommodate solder bumps instead of gold or aluminum wire ball bonds. An extra thick passivation layer is applied to the front of the bumped die to protect its active devices from environmental contaminants. Markings applied to the backside of the die indicate the die part number and its orientation.

Traditionally, flip chip attachment has been limited to the palladium silver or copper conductive traces on ceramic substrates. With escalating assembly pricing pressures making ceramic a less attractive choice. Possible substrates for substitution include polyimide film and copper foil laminates.

One impediment to COB has been the reluctance of chip manufacturers to ship ICs out the door without packages. Packages provide isolation and protection for the ICs and IC manufacturers make money on the packages.

Test and inspection of COB present problems associated with the lack of package leads, the high density of circuits in small COB systems and the close contact between chip and board. Advances in automatic optical inspection systems are solving some of these problems. Particularly

difficult is electrical in-circuit testing, in which comprehensive testing of dual-sided boards with line spacing under 10 mil is required.

Finally, COB is appropriate where the benefits of small size and high density outweigh the considerable technological barriers. In the late 1990s these barriers are likely to be overcome, making TAB the technology of choice for future electronic systems.

Right now multichip module technology is only affordable to manufacturers of high-cost, low-volume products. The long development cycles and higher development and manufacturing costs can only be justified at the high end. As cost and time-to-market improves, however, multichip-module technology will become a viable technology for lower-end systems.

For this to happen, however, a new breed of design tools is needed to reduce the cost and time associated with the development cycle. The traditional serial design approach with pockets of automation will not be acceptable if maximum performance and density are to be achieved.

The next generation of electronic design-automation tools must provide high-level design verification, synthesis, and partitioning tools that allow engineers to work at the conceptual level, thinking in terms of functions they want to implement rather than the actual physical mapping of their functions. These tools must also provide multilevel physical design instruments that are equally applicable at the IC, MCM-substrate, and board levels in a homogeneous environment. These design tools need to encourage multidimensional, constraint-driven design optimizations and trade-offs at various levels of a design's physical hierarchy.

Surface-mount technology challenges assembly engineers with a new set of manufacturing defects such as bent leads on quad flatpack ICs Inspection has typically been the least automated and among the most intransigent of the SMT assembly steps. Automated optical inspection (A( )It systems have been used to automate some assembly processes. As tine pitch SMT boards become more prevalent, fault detection with traditional X-ray in. optical tools has become more difficult. X-ray inspection systems, suitable for finding hidden defects, have improved in cost and throughput recently. Successful participants in SMT and advanced packaging markets will recognize and address inspection and test as important processes.

An important area for IC packaging is the area of material selection and processing. Based on these factors, rather than on die selection or system design, OEMs will be able to create unique, competitive products. The advantages achieved by using leading-edge packages can only be fully realized if proper materials and processes are also used.

While electrical performance advantages are possible with multichip modules, the packages themselves pose serious thermal management problems that must be addressed through proper material selection and package design. For example, the Fujitsu VP2000 uses a conduction cooling module that relies on an individual liquid impingement cooled assembly to contact each chip package. The chips are tape automated bonded into single micropackages and are in direct contact with the top aluminum nitride plate of this package. The chips are 1.35 cm square, and the aluminum nitride heat transfer plate is 1.7 cm square. The board of the module is multilayer ceramic and contains 61 layers for a total thickness of approximately 9.3 mm. The VP2000's mean total thermal resistance from the chip to the fluid is 0.56(degrees)C/W, of which 0.22(degrees)C/W is associated with conduction to the fluid and 0.34(degrees)C/W is associated with convection. The module was designed to cool 30 W packages and a total board heat load of 4.6 kW.

Heat dissipation is not the only consideration in material selection. There is also the problem of heat mismatch. When the thermal coefficient of expansion (TCE) between the chip and the substrate are different, a tendency exists for problems to develop during processing. Tombstoning is the most prevalent, wherein a chip stands up when heated. The perfect substrate for mounting chips would be silicon, since it would have the same TCE as the chips. Aluminum, gold or copper conductors can be deposited on

silicon through evaporation, sputtering or electroplating. This enables the conductors to be patterned by means of photolithography. Then thin-film dielectrics of polyimide or other polymers can be spun, sprayed or extruded onto the surface. The primary problem with silicon substrates is their high cost.

Advanced packages, such MCMs, are also placing new demands on the insulating or dielectric layers used for packaging chips. Based on electrical requirements, dielectric coatings for MCMs, for example, are thicker than those for semiconductors--usually with a minimum thickness of 10 microns. Preferred materials must exhibit low dielectrics, low moisture absorption, planarizing capabilities, and high thermal stability to accommodate subsequent processing.

Traditionally, morganic materials have been used to separate the last metal layer when interconnecting an integrated circuit. Generally limited to 2 microns or less, inorganic films reproduce the topography of the underlying substrate since they lack any inherent planarizing property. Thicker inorganic films are prone to cracking. The significance of these limitations is realized in manufacture of advanced semiconductors having three or more layers of metal interconnection. The step size and complexity of the underlying substrate increases with each successive layer, making it increasingly difficult to deposit a smooth and conformal film. Step coverage is poor and the coating can thin out over a sharp surface relief. This eventually leads to poor line width resolution and long-term reliability problems resulting from cracks and discontinuities. Polymers bring certain advantages with them when used as dielectrics in advanced packages. Although no one commercial polymer is currently able to meet all requirement s, polyimides have received a great deal of attention because of their demonstrated reliability as passivation and interlayer dielectrics in IC fabrication, plus their attractive overall balance of properties.

An Environmental Solution for Solder

Strong, easy to apply and capable of withstanding rugged environments, Ames Lab's new lead-free solder has a combination of characteristics that make it particularly appealing as an environmentally friendly replacement for tin-lead solder that often ends up contaminating landfills.

"We are interested in the capabilities of this new lead-free solder. It has a higher metallurgical strength than other solders presently available and other metallurgical properties that give it a long life," says Alan Gickler, general manager of Johnson Manufacturing, a solder manufacturing company planning to produce Ames Lab's new solder for use in the heat exchanger industry.

The worldwide search for an effective lead-free solder may be over as Ames Lab's new environmentally friendly option begins reaching the marketplace.

For centuries, tin-lead solders have been the standard for low-temperature bonding of metals, but now industry needs another choice. Hazardous to human health, lead in solder presents risks in the workplace and at the landfill where soldered electronic boards routinely end up. In fact, the U.S. Environmental Protection Agency has identified lead in discarded electronics as a groundwater contaminate, legislation has been proposed to eliminate lead from solder, and industry experts predict regulation of lead solder is on its way.

"While our solder is lead-free and reduces the environmental hazard, that's not its only advantage," says Ames Lab's Iver Anderson, co-inventor of a new solder from tin, silver and copper. "We worked with different alloy combinations and solidification processes to find a unique composition that retains many qualities of tin-lead solders but offers improvements too, such as greater strength and heat resistance," explains Anderson.

Testing solderability and strength, collaborators on the project at Sandia National Laboratory have confirmed that the new solder will apply easily like traditional solders yet offer increased strength important for

withstanding the rugged environments of today's high-tech applications. A slightly higher melting point, within the operating range of current soldering equipment, is another advantage of the new solder -- making it less likely to fail in high-temperature settings like under the hood of an automobile.

While other lead-free solders are under development, the availability and cost of the metals in this new solder coupled with its outstanding properties make it a particularly attractive replacement for tin-lead. Commercial solder manufacturers seem to agree. One company is already producing this new solder for use in heavy-equipment radiators while another is finalizing the licensing process to produce the solder for a different application.

Environmentally Friendly - Unlike traditional solder, Ames Lab's new solder contains no lead. It also contains no by-products of lead mining as some other lead-free options do.

Increased Strength - A finer microstructure allows this solder to withstand greater stress and more rugged settings, than traditional solders.

More Temperature-Resistant - Unlike traditional solders, this can withstand higher-temperature environments and the thermomechanical fatigue of dramatic temperature changes, both common in today's high-tech machinery.

Resists Corrosion - Unlike tin-lead, this solder is not sensitive to corrosion, which can weaken a soldered connection.

Easy to Work With - Like traditional solder, but unlike many other lead-free options, this applies to metals easily and can be formed into sheets or wires for accurate placement.

Inexpensive and Available - While slightly more expensive than tin-lead, the metals of this solder (tin, silver and copper) are abundant and less expensive than most other lead-free solders under development.

The strength, heat resistance, workability and cost-effectiveness of Ames Lab's new lead-free solder make it an attractive alternative for getting environmentally hazardous lead out of commonly used solders.

Solder Balls & Low Solids Fluxes

What follows are some thoughts and comments on a few questions concerning solder balls. We have done quite a bit of work in this area and have discovered several factors that have an effect on the occurrence of solder balls. To make a long story short, however, I believe that solder balls are here to stay for a while.

There are steps that can be taken which will reduce the number and size of solder balls.

Selection of Solder Mask

There have been well-documented cases of solder balls being virtually eliminated just by switching from one solder mask to another. Almost all of these cases have one thing in common. The former mask was a dry film type product while the latter was either a liquid photoimagable or wet film product. I believe that a difference here is surface tension as well as topography of the solder mask involved. Surface tension comes into play when one considers how well flux residues are held in place. Some residues are needed in order to reduce surface tension of the solder as it peels away from the PWB assembly. Rough surface finishes on the solder mask have, in general, displayed significantly fewer solder balls when compared to high gloss surfaces.

Several "Matte" finish LPI and wet-thermal cured solder masks have been introduced to the market. This rough topography of the solder mask may give flux residues a "foothold" to stay in a desired area.

Flux Selection

Flux selection does have some play as to the occurrence of solder balls. A rule of thumb is that the lower the solids content of the flux is the more solder balls will be noted when all other parameters are held constant. This is sort of a dilemma for us as a flux manufacturer in that if we increase the solids content, we will more than likely have an adverse

impact on probe testing of final soldered assemblies. The aesthetics of the final soldered assembly will also be affected as you can imagine.

Solder Mask Cure

There have been reported cases of increased solder balls due to insufficient cure of solder mask. The effects here are probably tied to producing PWB's with different surface tension characteristics.

Humidity of the Soldering Environment

I have no scientifically backed explanation for this. It has been reported several times that as the humidity of the production environment increases the occurrence of solder balls also goes up dramatically. One manufacturer I have worked with will stop production if the Relative Humidity rises above 55%. The only hypothesis to date that makes sense is that humid air around the solder pot will change the surface tension characteristics of the solder at the peel off zone. More work needs to be done in this area.

Design Considerations

There are several PWB design considerations that have proven to have an effect on the occurrence or absence of solder balls. It has been our experience that the majority of solder balls are located between two closely spaced leads. It is interesting to see a DIP pack or edge connector that has one solder ball located in the center of each pair of two leads. It is very difficult to explain why these occur in writing. We believe that it has to do with how the solder drains from two adjacent leads. Imagine a web formed between the two leads that drains upward towards the board surface. When the web breaks, it doesn't do so cleanly if the area has little flux present to reduce surface tension, a solder ball is left in the middle.

The adhesion mechanism is surface tension related.

With this explanation in mind, the following statements appear to hold true in the field.

The further apart two leads are from each other, the less likely a solder ball will be formed between them.

Decreasing the area of solder mask that is present between two leads that typically show solder balls will decrease the occurrence of solder balls. In fact, it has been demonstrated that complete removal of solder mask between leads eliminates solder balls.

The sharper definition of the solder mask the more likely solder balls will occur.

The rougher the surface of the solder mask, the fewer the solder balls.

As the distance of lead protrusion from the bottom of the board decreases so does the occurrence of solder balls.

Solder Balls Caused by Pallets, Fingers, and Clips

Another unrelated type of solder ball that can be noted are those that occur close to the conveyer fingers, around pallet fixtures, and behind clips or stiffners used to support the board or to protect gold fingers from the solder bath. These type of balls are, upon closer visual examination, actual solder captured in dross in most cases. As the conveyor fingers do not see any great quantity of flux they may pick up small amounts of dross with each pass over the wave. Without a well-maintained finger cleaner, the dross will build up with the flux residues until it reaches an amount that the individual finger can hold. If this is released in the wave as the board is submerged, it is possible that this dross will be deposited on another area of the board. The same idea holds true for the other fixture devices mentioned.

The remedy for this type of solder ball is to maintain clean equipment and fixtures. For the Kester product that you have worked with I recommend a 25% water 75% isopropanol mixture in the linger cleaner. Regular changouts of this solution will be dictated by the operating time of your equipment. Pallets can be designed so that there is support of the board without intimate contact around the entire perimeter. This minimizes flux entrapment which can lead to outgassing in the solder wave as well as

extending the number of cycles a pallet can go through the wave before having to be cleaned.

Electrical Testing Interference Caused by Use of "No-Clean" Fluxes

Most high volume production facilities rely on fast testing of the final soldered assembly. One of the most popular methods used is "bed of nails" testing. Since the introduction of "no-clean" fluxes to the market, there has been increased concern as to the compatibility of an uncleaned solder assembly with the electrical testing process. There have been different occasions where interference with "bed of nails" testing has been reported with the use of "no-clean" flux product.

The construction of the printed circuit board has a direct bearing on successful testing at the bed of nails station. Single-sided boards with punched holes have been implicated as the main culprit on several occasions when interference was noted while using a no-clean manufacturing process. These boards have a high level of laminate debris left on them from the punching process. This debris is loose and easily dislodged at the fluxing station only to be redeposited on a different location on the same or subsequent assembly. Examination of the flux tank after several hours of production use will show a high level of insoluble particulate matter that has been washed off of the boards. After soldering using a no-clean flux, the final assemble is no longer subjected to a wash cycle which previously would have removed this particulate laminate material along with the flux residues. Instead, it is left in place on the bottom of the soldered assembly. If the laminate material, being non-conductive, gets between the test pin and the test pad, and "open" defect is noted by the test equipment. Chances are the next board tested will not show an open in the same location. As the particulate matter in the flux tank accumulates, the occurrence of false "opens" at the test station increases. In an extreme case, the particulate board laminate material concentrates at the head of the test pin itself, causing a consistent false "open" test defect.

There are several test pin styles available on the market. Sometimes decisions are made on price with no regard to the quality of the test pin itself. There are several considerations involved in selecting the proper pin style.

Selection of test pin type should be made carefully using the test equipment manufacturers recommendations. In general, it has been noted that lance type (single needle point) pins out-perform other styles. At 8-oz spring pressure, there is enough force to penetrate the surface of a soldered test point. Gold properly alloyed with another metal gives better wear characteristics than 100% gold plating. Finally, test pins having lubricant should be avoided, as this will allow debris to stick to the pin.

Different process parameter settings in the wave soldering area when using no-clean fluxes can lead to different results at the electrical testing station. Probably the most important parameter to control is the percent solids in the flux. Specific gravity controllers do not do a sufficient job on fluxes having solids contents of 5% or less.

Obviously, the higher the solids content the more residues will be present on the soldered assembly that is being tested. No-clean fluxes are best monitored using a direct method of measurement such as an acid number determination. Use of the PS-20 Test Kit for the 920-CXF and 922-CXF "No-Clean" Fluxes does an excellent job of controlling the solids content when used properly. The PS-22 Test Kit is recommended for non-foaming versions, #920-CX and #922-CX.

Other line parameters should also be controlled tightly. This is more because of solderability issues than for decreasing interference at the bed of nails station. It is interesting to note, however, that on some assemblies there seems to be a decrease in the amount of visual residues as the preheat temperature is increased. This may have an effect on electrical testing interference.

With the Kester "No-Clean" formulas, the recommended preheat temperature is 210-230(degrees)F Above this range, little differences in appearance can be noted. Dropping the preheat temperature below

180(degrees)F on the topside of the board will usually result in dull looking solder joints. Even still, the residues present causing this dull appearance are easily penetrated by the electrical testing pins.

Different fluxes can be expected to produce different residues having varying effects on bed of nails testers. Fluxes that produce excessive residues on the test pads and solder filets should be avoided. The residues should be dry and tack-free upon exit of the solder wave. Residues should not be allowed to accumulate on conveyor fingers. If pallets are used, they should be washed on a regular basis. Kester's "no-clean" fluxes will not result in excessive residues being left on the soldered assemble. Compared to our competitors products, you will find, in most cases, a great reduction in the amount of residues left on the soldered assembly.

In most cases, an electrical test pin in a bed of nails tester is lined up to make contact with a test pad instead of actual contact with a soldered lead end. These test pads can be compared to surface mount pads in that they do not have plated through holes associated with them. Wetting properties of the flux have to be good in order to solder these pads. This is important in that when a test pad accepts solder, the solder will displace the flux residues to the outside of the pad. If the pad does not wet with solder from the wave, displacement of flux residues does not occur. This can be especially detrimental to bed of nails testing if the flux is heavily laden with the aforementioned particulate board laminate material. A manufacturer should require a flux to have a high level of wetting activity. All of the Kester "No-Clean" formulas will provide wetting within one second of contact with the solder wave. This will ensure total coverage of all test pads, especially with a dual wave soldering pot.

Preventative maintenance measures can be incorporated into the process once it is understood what is causing the process to exceed control limits. The following is a list of maintenance suggestions which will reduce or eliminate interference at the bed of nails test stations.

If PWB's are single-sided, require they be washed as a final step by the vendor in order to reduce the amount of loose board laminate debris. Change the flux more often or filter frequently if insoluble matter builds Evaluate current choice of test pin as to compatibility with present process. Keep percent solids content of flux in check using an acid titrate method. Test pins may need to be brushed occasionally. The test fixture may need to be vacuumed on a regular basis depending on accumulation of debris within the fixture. If pallets are being used to hold assembly, they should be cleaned on a regular basis. Wave solder machine should be cleaned on a regular basis.

Alternatives to Solvent Cleanable Solderpaste

The upcoming reduction and elimination of CFC-113 use is changing the way that Kester approaches solderpaste development. In the past, RMA solderpaste formulas were strictly designed to be solvent cleanable. Today, because of the uncertain future of solvent cleaning, solderpaste vendors are looking at significantly different formulations.

Although it is too early to predict which direction the electronic assembly industry will choose as a long term solution in eliminating CFC-113 use, some trends are starting to develop. These trends can be broken down by the different segments of the industry; computer, telecommunications, automotive, consumer and military. One may argue that these segments overlap, but there appears to be a definite distinction in the way companies within the segments perceive their needs. Whether such distinctions should exist is not relevant in the short term. The long term stated goal of the entire industry is to arrive at a "no-clean" process. Two things make this difficult to achieve for reflow soldering.

First, there is a common perception in the industry (mostly in the U.S. computer and military segments) that a circuit board is not reliable unless solder joints are bright and shiny and the circuit board is entirely free of flux residue. Long term reliability studies performed tin the telecommunications industry have implied this is not the case. Some RMA flux residues can be as safe when left on the circuit board as when

removed. This issue becomes one of perception, rather than fact and may disappear if the need for eliminating cleaning becomes great enough.

The second and more powerful issue stopping users from leaving solderpaste residue on the circuit board regards the creation of solderballs in the assembly process. Solderballs may or may not present a reliability risk depending on their size and location on a circuit board, but it is considered safer to wash off any that form. Many solderpastes are capable of reflow without forming solderballs, but the reflow assembly process is not capable of solderball free operation. Many factors influence the creation of the solderballs including: circuit board quality, pads design, component type, mask height, print alignment, stencil design, stencil quality, print parameters, placement pressure and reflow profiles.

At present, one may be able to approach the total elimination of solderballs on 50 ml pitch and coarser circuitry, but the currently allowable material and process tolerance are too great for errorless fine pitch assembly and at least a few solderballs will occur.

Kester's Direction of Development

Since it appears that several different directions will be taken by solderpaste users, Kester will be developing solderpaste product along the various paths concurrently. A breakthrough may occur which will favor one particular direction, but that is not apparent at the present time. Such breakthroughs may include:

A water soluble flux residue which does not affect surface insulation resistance, even when left on the circuit board.

A method of cleaning solderballs off a circuit board without using a current cleaning method.

A uniform assembly process which guarantees the elimination of solderball formation.

A new, environmentally safe and non-hazardous solvent which is compatible with circuit board cleaning.

A method of component attachment which replaces solderpaste and reflow.

Development Progress

Saponification with RMA fluxes

Certain RMA fluxes can be easily cleaned using an appropriate saponifier and water cleaning system. Kester #5779 works well with the Kester formulas designed to be saponified. The advantage of using an RMA solderpaste with saponification is the fairly safe, standard flux which does not affect board reliability.

The disadvantages include the need for water cleaning equipment, water treatment equipment for effluent and the unknown effect of saponifier on common circuit board materials. Although saponification has been used in the electronics industry for many years, it has not been widely used in high volume surface mount applications, particularly with fine pitch components. Those companies using saponifier for solderpaste reside removal have experienced some difficulty removing residue, although reliability does not appear to have suffered.

Kester is in the process of developing RMA solderpastes which contain fluxes specifically designed to be removed with amine based saponifiers. New formulas R-236 and R-250 can be cleaned in a 3-5% saponifier solution and provide the safety of traditional RMA fluxes.

Water soluble OA solderpastes

Water soluble solderpastes eliminate the need for a rosin saponifier in the water solution. Until recently very little work has been done with them regarding both safety and reliability. The traditional problems with OA solderpastes have been an inability to print well, reduced tack life, poor reflow after several hours from printing, reduced cleanability and reduced surface insulation resistance.

It is likely that these problems will be worked out in the near future. In fact, Kester has been able to eliminate most of the problems with a new series of water soluble solderpaste including R-572. The major problems of the conductivity of residue, S.I.R. degradation even after

cleaning and reduced reflow capability in humid environments may be long term problems which will never be solved.

Typical RMA flux residues yield S.I.R. values in the range of 1012 ohms/square in either the cleaned or uncleaned state, when tested using the IPC comb pattern test method at 50 C and 90% humidity. Most OA fluxes have S.I.R. values in the range of 109 ohms/square when cleaned and 106 ohms/square uncleaned. It is not certain whether this lower S.I.R. is satisfactory for the new types of circuitry being developed or whether higher clock speeds and lower voltages will require higher insulation resistance.

Another problem is that new solderpaste manufacturers or those not having the capability of doing the necessary reliability work are coming out with water soluble products which may not be adequately tested and their customers may not be aware of the risks.

Kester's most recent water soluble solderpaste formulas (R-572 and related products) have S.I.R. values in the mid 1010 ohm range when cleaned in a beaker, per the IPC method and above 1011 ohms/square when cleaned in an automated in-line cleaner. The uncleaned residues still yield unsatisfactory S.I.R. values, but the higher cleaned results are promising.

No Clean Solderpaste

No clean solderpastes would be the best solution of all. There would be an overall reduction of cost with no loss of reliability or risk to the environment. The problem is the surface mount process. It is virtually impossible to assemble a circuit board without creating at least one solderball. Without cleaning, there is currently no way to remove that solderball and it may pose a reliability threat later on.

We envision "no clean" solderpastes as having a cosmetically acceptable residue which does not pose a reliability risk and can be cleaned if necessary.

Kester is working with modified rosins which have a higher than normal melting point and insulation resistance. One such resin which has been incorporated in the halogen free Kester R-236 solderpaste has a melting point of 120 C. Typical grade WW rosin softens at approximately 65 degrees C. The higher melting point gives a larger operating temperature window before the flux becomes active, conductive and corrosive.

No Residue Solderpastes

Although Kester has attempted to develop a practical version of this type of solderpaste in the past, the idea has been temporarily shelved. Other pastes which are touted as "low residue" paste have turned out to be ineffective and as yet no viable product has been brought to the market. We may pick up this research in the future after we develop successful water soluble and no clean materials.

Advice to those customers trying to decide on a course of action:

Reducing and eliminating CFCs is both ethically and economically advisable.

Depending on a company's current and traditional CFC consumption, both costs and availability may be affected.

Even by shifting the bulk usage of CFCs away from bottom side cleaning and toward top side solderpaste residue cleaning one is still not protected as supplies become tight and the possibility of an all-out ban exists.

Whether "no clean" production is currently practical or not, it is a good goal to aim toward. Before it can happen, however, much work has to be done to control the processes, raw materials and assembly components.

Similarly, water soluble materials have a lot of promise, but ground work still must to be done to improve water soluble material and cleaning equipment. Water soluble solderpastes are useless unless it can be guaranteed that all of the residue has been removed from circuitry.

We believe that now is the time to be involved in process capability studies to determine what electrical and physical requirements are necessary for the elimination of CFCs. Pressures to reduce CFC emissions may come sooner than expected and industry wide standards may not develop

in time. Delaying action can only be more costly.

The Effect Of Metallic Impurities On The Wetting Properties Of Solder

Since the development of wave soldering machines about twenty years ago, the electronics industry has become more aware that certain metallic impurities have and effect on the wetting properties of solder. Traditionally the maximum amounts of contaminating metals -- such as copper, gold, antimony, iron, zinc, aluminum and cadmium -- have been established by trial and error over many years. There is a need in the industry for substantiated data so specifications can be established for replacing contaminated solder at the proper time.

This paper is a report of a continuing extensive study made to determine the maximum allowable impurities in solder used for wave soldering applications. This preliminary report concludes with a list of impurities compiled from actual analyses of solder which caused production problems. Still in progress is Phase 2 of the investigation which will report the effect of impurities in terms of spread, appearance, speed of wetting and amount of solder being used to complete soldered joints. A concluding list of recommended maximum allowable impurities will assist in establishing reliable quality controls on the purity level of the solder in a wave soldering machine.

With the introduction of wave soldering machines in the late fifties, the printed circuit industry moved into the age of automation and high productivity. Like any new process, there was a period of trial and error which extended over several years to determine the operating parameters of the equipment. The technician or assembler using a hand soldering iron had much better control over the soldering situation since he could control join-to-joint heating to complete properly soldered connections. Heating on the wave soldering machine, however, could not be variable if automation and productivity were to be accomplished. All joints were exposed to the same amount of heat, and only the mass of component parts being soldered determined the temperatures to which the surfaces were heated. The wave soldering machines and the problems associated with them helped advance soldering technology since the speed of soldering required more careful control of the other parameters for soldering. Studies began and still conti nue on the solderability of surfaces, the proper application of flux faster acting fluxes, types of preheating and conveyor mechanics. The temperature of the solder pot rather quickly was established at 60-80 degrees C higher than the melting point of the solder. This, like other parameters, was by experimentation. By far the most commonly used solder alloys were, and still are, 63/37 and 60/40 tin/lead. These alloys are low melting, bond to copper surfaces most readily, and melt over a narrow temperature range. There are many soldering fluxes to select, but after the choice is made, control is fairly simple by checking density and adding the correct amount of thinner.

At that time, twenty years ago, experience started to dictate that certain metallic and non-metallic impurities in the solder had an effect on the wetting properties of the solder and the amount of reworking of defective joints. Automatic wave soldering machines incorporate large amounts of molten solder which picks up contamination by a washing action of parts being soldered. Assuming that solderability and flux are under control, the only other factor that can have a serious effect on soldering quality is contamination in the solder. The speed of wetting is the single most important factor in automatic wave soldering since as many as 200 joints can be completed in one second. Any impurities which cause the solder alloy to become sluggish could result in icicles and shorts since the solder does not properly drain off the board as it exits the solder wave. Impurities which form intermatallic compounds with the tin or lead can cause gritty looking solder and make solder too sluggish to properly fill plated thr ough holes in circuit boards.

Investigations have been made to determine the metallurgical changes made on bulk solder by adding large amounts of impurities. These studies, however, were very generalized and not specifically related to wave solder.

Reports 1-3 vary considerably as to the permissible amount of contamination contained in solder before soldering problems might occur. These investigations were done before wave soldering developed into the scientifically designed process that it is today. Original machines soldered at speeds less than a meter/minute, while today it is not unusual to see conveyors moving 4-6 times that fast. The report by the Tin Research Institute in 1975 was very comprehensive and provided valuable information on the effects of impurities on the wetting ability of solder. Nevertheless, this study was not specifically directed to wave soldering and the results do not entirely agree with the percentages of impurities establishes over twenty years by trial and error.

The purpose of this paper is to summarize the traditionally accepted "trial and error" maximum allowable impurities, and then by testing under laboratory controlled conditions to establish maximum allowable percentages of contamination in solder used by the electronics industry. The effects of adding certain metallic impurities to 60/40 Sn/Pb solder will be reported in terms of wetting ability, spread, appearance and the amount of solder being used to complete soldered joints by wave soldering.

Source of Impurities

Though the purpose of this testing was to determine the effect of impurities dissolved during the soldering process, it is important to note that national specifications for solder are not strict enough to assure obtaining high purity metal. Secondary or refined metal could contain excessive impurities and shorten the usable life of the solder bath. Impurities such as copper, antimony, zinc and aluminum have an effect on soldering quality and should be kept to a minimum. Assuming that high purity solder is being used, the impurities are introduce into the solder from parts being soldered, from holding fixtures and from the solder pot itself.

Copper - Nearly everything on a printed circuit assembly is made of or plated with copper which dissolves rather rapidly in solder. The circuit board itself, component leads and jumper wires all introduce copper into the solder in a wave soldering machine.

Gold - No longer used as an overall protective plating, gold is used on certain component leads such as nickel-iron alloy used to make transistors, diodes and integrated circuits.

Cadmium - Sheet metal chassis frames and other parts might be cadmium plated to prevent rusting and improve appearance and solderability.

Zinc - Brass is an alloy of zinc and copper, so brass terminals, lugs and bolts are sources of impurities.

Aluminum - Fixturing devices, bolts and fabricated metal parts might be made of aluminum. The tough oxide film on the aluminum will usually prevent solder wetting; but with multiple solder immersions or if abraded, aluminum can dissolve in the solder. It is doubtful that aluminum will remain in the solder under production conditions since it will dross out when combining with copper, gold or antimony.

Silver - Many parts are silver plated to preserve solderability. Like the other coinage metals, gold and copper, silver will dissolve in the solder.

Iron - Temperatures over 430 degrees C will cause the solder to dissolve iron from the solder pot itself An improperly alloyed solder using too much heat could contain excessive iron. A new solder pot -- whether cast iron, cold-rolled steel or stainless steel -- will have exposed iron available for dissolution into the solder. Excessive cleaning of the pot walls with a wire brush can also introduce iron into the solder. The problem associated with iron contamination is excessive drossing which usually clears up as the iron compounds are removed with the dross.

Sulfur - It is very unlikely that sulfur would contaminate the solder bath during normal production. Sulfur might be present in secondary metals since it is used to remove copper during the refining process. Sulfur should be limited by national solder specifications to avoid its presence in solder.

Phosphorous - The main source of phosphorous is copper that has been deoxidized with phosphorous.

Problems Associated with Impurities

Phase I of the investigations involved a compilation of analyses performed over the last ten years for the specific purpose of solving soldering problems. The amount of impurities in the solder was related to observed defects or solder conditions. These defects, specifically cause by contaminated solder, are noted below with some discussion about the impurities which caused the problem. The table following this discussion shows the percentage range of impurities which seemingly caused the observed soldering defects.

Icicles, Shorts, Bridges Cadmium, zinc and aluminum in trace amounts increase the surface tension of the solder to cause this defect. Copper and gold increase the solder viscosity to cause the same problem.

Large Solder Fillets Copper, gold and antimony increase the melting point of the solder and the intermetallic compounds with tin or lead make the solder more sluggish. The result is larger fillets and more solder consumed to create the solder joint.

Unfilled Holes

The speed of wetting is reduced by the presence of copper, gold, antimony and cadmium. Though no instance occurred with zinc and aluminum, these metals are likely to also affect wetting speed because of their ability to increase the surface tension of the solder.

Dull Solder, Gritty Solder

Cadmium and zinc in trace amounts make the solder surface dull. Gold also dulls the surface but is quite often indicated by a sparkling, crystalline surface condition. Bismuth or antimony in large amounts above 2.5% also dull the surface. Copper and aluminum contamination result in a gritty-looking solder surface. Both phosphorous and sulfur have caused gritty solder though rarely are these two impurities found in solder samples.

Dross inclusions in the solder show up as visible particulate grit or hidden inside a bump or pimple in the otherwise shiny solder surface. Quite often the source of this problem is an unusual amount of iron in the solder.

Cracked Joints

Inclusions in the solder such as intermetallics of tin or lead with copper, gold and antimony can provide the nucleus for crack propagation.

Dewetting

Zinc, antimony and phosphorous can cause solder to dewet on copper.

By looking at the real world of wave soldering and the ten years of analytical records, we can summarize the impurity levels which traditionally caused problems.

Immediately obvious by an examination of this list is the fact that the percentages established by experience are not precise numbers. The explanation for this is that the defects cause by the impurities may be acceptable at one company and cause for rejection at another company. Rigid inspection requirements for aerospace or military products might reject solder joints which are acceptable for consumer products. Difference between fluxes, soldering machines, circuit board density, component layout, hole sizes, solderability and amount of heat all contribute to the quality of soldering.

Soldering Electronic Assemblies

The soldering process is a total system of interrelated factors involving solder, flux, solderability and heat. The reliability of an electronic assembly is directly related to the quality of the soldered connections. This paper discusses the basic principles of soldering and what controls are necessary to achieve high quality and productivity.

The development of the electronics industry is closely related to the ease of joining metal surfaces with solder. There is no more economical way than soldering to make reliable electrical connections. The extensive use of the printed circuit board was made possible by the ability of solder to

metallurgically bond the electronic component leads to the circuit board conductors. The reliability that must be built into electronic assemblies is directly related to the quality of the billions of soldered connections make every year.

The failure of an expensive or vital piece of electronic equipment can frequently be traced to a defective solder joint, a costly error made by an assemble or soldering operator with an inadequate understanding of the principles of soldering. Soldering of electrical connections involves scientific techniques and practical experience. The science of solder metallurgy and the chemistry of soldering flux are carefully researched in solder manufacturers' laboratories, resulting in high-quality products for every soldering application. The user of soldering materials should become familiar with the basic requirements for making reliable soldered connections and develop the necessary skills in using the proper solder, flux and soldering equipment. Whether soldering by hand with a soldering iron and flux cored wire solder or with automated soldering machines, there are only four important factors to understand.

Every soldering application involves these four factors, all equally important in the process of completing reliably soldered assemblies. Circuit board metal surface, type of plating, protective coatings and layout should be selected with soldering in mind. Component lead solderability and placement on the circuit board in a solderable configuration also will determine the reliability of the soldered assembly. The choice of soldering flux is directly related to the solderability of the metal surfaces. Solder alloy, selection and the level of purity will determine the speed of soldering.

Solderability

Many definitions have been given for the term "solderability" which simply means the ability of the metal surface to solder properly. Solderability can also relate to the design and layout of the printed circuit board. Pad configurations, circuit paths and component placement should all make automated soldering easier and more reliable. Solderability also pertains to the selection of metal surfaces which will solder easily. The solder must be able to flow out quickly on the surface, forming a uniform, molecular bond between the surface and the solder.

Solderability should be the prime consideration when selecting materials, designing the circuit and fabricating the component parts and circuit board. Modem electronic assemblies are too densely populated and too small to inspect for defective solder joints caused by poor solderability. Only by using solderable parts and maintaining good soldering process control can the objectives of high quality and productivity be achieved.

There are many soldering defects that are not related to the solderability of metal surfaces. For instance, production requirements may specify that a single-sided board must be drilled with all the same size holes to reducer the cost of the board. Unfortunately, component leads are not all the same size and bridging solder across a large hole to a small lead becomes difficult. Drilling procedures should not leave a raised edge or burr around a hole. Solder, like any liquid, has a high surface tension arid does not flow easily over a sharp edge. Also, non-metallic materials may contribute to soldering defects. Improperly applied solder mask may get into plated holes and prevent soldering. Solder might stick to uncured solder mask or glass epoxy.

Copper is selected as the printed wiring on circuit boards not only because of its good electrical conductivity but also because of the ease of soldering. Clean copper is very solderable. Even without flux a fairly clean copper surface will wet with solder when dipped into a solder bath. Figure 1 is an illustration of a copper surface which has been soldered.

Soldered Copper Surface (cross-section)

The tin in the solder actually does the bonding as the solder penetrates the grain boundaries of the clean copper surface. At the solder-copper interface, two copper-tin intermetallics form rapidly during

the heat of soldering. Typically, the thickness of the intermetallics is about 0.25 microns (10 micro-inches). The formation of the intermetallic compounds Cu6Sn5 and Cu3Sn is indeed and indication that molten solder came in contact with clean copper metal; but the quality of the solder-to-copper bond can deteriorate if the intermetallic layers are too thick. If the copper-tin intermetallics exceed a thickness of 0.50-0.75 microns (20-30 micro-inches) the solder will no longer adhere and the result is dewetting.

Therefore, the amount of time that the solder is melted on the copper becomes very important. All soldering should be done rapidly so that the melted solder is contracting the metal being soldered for a minimum amount of time. When people specify thick fused (reflowed) solder coating on copper, they assume that the shiny solder surface exhibits the good solderability of the circuit board. We cannot make such an assumption since the solder may have been melted too long at too high a temperature. Quite often a circuit board that has had the solder plating fused or melted in a infrared heated oven may exhibit a shiny solder surface which actually conceals an already excessively thick copper-tin intermetallics layer. On subsequent melting of the solder coating during the soldering process, the solder dewets when the intermetallic layer thickens. Never conclude that any surface is solderable until alter a solderability test is run.

The best surface to solder is bare copper. Any coating applied to the copper surface should not inhibit solderability.

Metals, such as copper circuit boards and nickel-iron component leads, must be cleaned of surface contamination (such as oxides, carbonates, sulfides, oil) before plating or coating. Tin, solder, silver, gold and rosin coatings will deposit over dirty base metal but also will dissolve away during soldering. The result will be defective, poor quality soldering since solder cannot bond to dirty surfaces.

Whatever type of surface is selected for soldering, fabrication of the printed circuit board and component leads should be controlled by testing solderability prior to assembly and soldering. Only a clean surface is a solderable surface.

Various Degrees of Solderability

Solder surface is smooth, bright and completely covered. Solder does not flow and leaves exposed base metal.

Solder withdraws from areas leaving a thin film without exposing base metal.

Wetting - A surface is wetted when the solder flows well, forming a continuous, unbroken film, free of pinholes and depressions.

Non-wetting - Areas of the base metal are visible through the solder coating. The contact angle between the solder and the base metal is very large and there are distinct boundary ridges. Non-wetting is most common on circuit boards with overcured rosin protective coating that acts like an epoxy barrier since it does not dissolve in the flux. Solder mask that bleeds into plated holes in a circuit board is another cause of non-wetting. Metal surfaces also can non-wet. Thin tin or solder coatings (0.25 microns) are rapidly migrated through by copper, resulting in a non-wettable copper-tin intermetallic surface. Brass quite often is coated with immersion or electroless tin, and after migration occurs, the copper-tin intermetallic coating is covered with zinc oxide. Certainly this cannot be soldered with a mild rosin flux. Nickel-iron component leads are often non-wetted but the situation is difficult to see because nickel-iron is the same color as solder.

Dewetting - The solder appears to have wetted the surface but then immediately pulled back from areas leaving an irregular, lumpy coating. Dewetting is more common than non-wetting but not a much different situation. The intermetallic formation just described as non-wetting can also be the cause of dewetting. If a copper surface is exposed to molten solder for too long a time, either continuously -- during manufacturing -- or repeatedly -- during unnecessary rework or touch up -- the copper-tin intermetallic thickens and the solder pulls back leaving a dewetted surface. Copper is a soft metal, and hard particles such as pumice or

aluminum oxide grit can be ground into the surface during improper cleaning procedures. These trapped particles do not wet with solder and the inclusions inhibit proper wetting of the copper. Additives such as brighteners or leveling agents in the copper or solder plating baths cause dewetting when an excessive amount is codeposited with the plating. Most "bright" plated surfaces wil l cause soldering problems such as dewetting or outgassing. If plated through holes are being used in a printed circuit board, the plating baths -- copper, tin, solder -- should contain minimum organic and metallic impurities since these unsolderable materials deposit in the area of lowest current density, in the plated through holes. Then, the soldering problems such as dewetting and blowholes are built into the circuit board. The solderability of component leads is also affected by organic brighteners in tin or solder plating since the resulting outgassing may not be detected by a solderability dip test. However, the outgassing will cause blowholes when the component lead is soldered into a plated through hole in a printed circuit board.

Solderability Does Not Just Happen - The supplier or manufacturer of the printed circuit boards or component should be building these parts to the specifications of his customer. If a company has no specification describing exactly what is desired in dimensions, coating, thickness and solderability, that company is taking a chance that the boards will not solder properly, manufacturing productivity will go down and product quality will deteriorate.

Solderin Flux

Soldering flux is only one part of the total soldering system, but the choice of the proper flux and the correct use of that flux can directly determine the reliability of the completed electronic assembly. Soldering flux is simply the environment in which molten solder must work. A metal surface which is coated with flux is in a state of change -- a change from a passive, contaminated surface to an active, clean surface. The soldering flux, whichever type is used, must prepare the metal surface for the solder.

Solder is not a glue which simply sticks two surfaces together. Solder is not just a filler metal which is used to fill space between two metal surfaces. Figure 3 shows schematically how solder will wet and spread on a clean metal after flux has done its job of preparing the surface by removing oxides and tarnish. Without flux the solder would pull back from the dirty surface into an elliptical shape, much as water balls up on a waxed surface.

Effect of Flux of Wetting

Only when the surface is clean will the adhesive bonding forces between the solder and the metal surface overcome the solder internal cohesive force, causing the solder to flow out on the surface. During the heating process the flux provides a barrier, insulating the metal surface from oxidation by air. Acting as a wetting agent, the flux then causes the solder to flow out on the clean surface, forming a bond. The choice of soldering fluxes can only properly be determined by the degree of solderability of the parts being soldered. Unfortunately, many times the solderability parameter is separated from the reasons for selection of a particular flux. The choice of flux may be made for some property such as solvent content, flash point, odor, water or solvent solubility, conductive or corrosive characteristics, price or any other reason. Far too often a company will take and unorganized approach and try every flux made in an attempt to find that one magic formula which accomplishes the ideal soldered connection.

A very simple rule for selecting a soldering flux is that clean metal surfaces solder with mild fluxes. The stronger a flux has to be to remove metal oxides, the more corrosive the flux becomes and the more important it is to remove the flux residue. For electronic applications only the fluxes based on rosin are considered "safe". Because rosin solidifies as a glass, the insulation resistance is very high, at least equal to the printed circuit board material of about 1012ohms. Rosin is derived from pine tree

sap and consists of a complex mixture of water insoluble organic acids, primarily abietic acid.

Though relatively inert at room temperature and still a good insulator at 85 C, rosin is active enough at soldering temperatures to remove oxidation on copper. This fairly good fluxing ability and the inactivity after soldering have made rosin-based fluxes the standard in the electrical industry for over seventy years. When the electronics industry began to automate by using machines to solder printed circuit board assemblies, plain rosin flux was not active enough to clean the metal surfaces as rapidly as required. Activating agents which are capable of releasing small amount of hydrochloric or hydrobromic acids during the heat of soldering are added to rosin fluxes to make them more active and efficient. Other organic acids, which are stronger than rosin, are sometimes added to rosin fluxes to improve the fluxing action. Most activators also improve the ability of the rosin to withstand the soldering temperatures without decomposing excessively.

Rosin fluxes vary by the amount and type of solvent used as a vehicle for the rosin. The solvent used in rosin flux cored solder wore makes the flux flow out faster and promotes more rapid spreading of the solder. The trend today with liquid fluxes is to use activated rosin fluxes with a low solids content in the range of 10-20% solids. These new fluxes have been developed for modern wave or drag soldering equipment and, unlike the more concentrated rosin fluxes in the 25-50% solids, range, leave minimal residue after soldering. Many companies, in fact, choose not to remove the small amount of insulating residue or, at the most, will remove flux residue only from the bottom of the circuit board with in-line rotary brush cleaning equipment.

Soldering flux is only left on the circuit board assembly if the rosin residue is hard and non-tacky. To get this dry residue requires the use of alcohol solvent systems which evaporate during soldering. Other solvents such as mineral spirits, glycol ethers and terpenes evaporate slower, resulting in a sticky, more conductive residue without good insulating properties.

Other organic acids which are water soluble, unlike rosin which is soluble in solvent but not in water, are used as soldering fluxes particularly in the computer industry. If components on the circuit board are positioned so that thorough cleaning with water can remove all of the flux residue, the organic water soluble fluxes can be used. These fluxes are corrosive and leave electrically conductive residue. The large volume of water (10-20 liters per minute) required to remove the flux residue sometimes prohibits the sue of organic water soluble fluxes unless the water can be recycled.

Flux Removal

With the choice of new fluxes available to the electronics industry, many companies are reviewing the need to remove flux residue at all. The low solids rosin fluxes are being left on the circuit board assemblies or, as many companies do, removed only from the bottom of the circuit board.

Solder

If the metal surfaces have been properly cleaned and coated with flux and heated to the correct temperature, nearly every solder allow will bond to the metal. Though there are hundreds of solder allows made form many different metals, the most common solders consists of a mixture of tin and lead. For electronics soldering only the alloys near the eutectic composition of 63% thin and 37% lead have the required properties.

For most wave soldering applications, 60/40 alloy is preferred. The rapid wetting action, low melting point and minimum melting range are favorable to the wave soldering process. For single sided circuit boards, the plastic melting range of 60/40 alloy helps the solder bridge across larger holes with small leads, resulting in fewer voids to touch up. For plated through hole circuit boards, especially those with small 1-millimeter diameter holes, 63/37 alloy because of its better capillary action can better fill the holes than 60/40. Other alloys with lower tin

percentages have been used for wave or drag soldering but the small amount of material savings is offset by the increase in expensive touch up or rework. Even for soldering by hand, the 60/40 alloy permits so much more rapid soldering than the higher melting 50/50 alloy that 60/40 is the industry standard. The 62/26/02 TIN/LEAD/SILVER alloy is for special applications where surfaces being soldered are plated with silver or silver-palladium. Ceramic chip components and ceramic hybrid microcircuits are soldered with this alloy containing silver so that the silver metallizeation is not dissolved by the solder.

Effect of Impurities in Solder

Metallic impurities such as copper, gold, cadmium, zinc, and antimony and non-metallic impurities such as oxides and sulfur have a combined effect of lowering soldering efficiency. Contamination increases the viscosity of the solder, causes surface oxidation and increased surface tension, causes large solder filets, more solder per connection and bridging between circuits. A regular analytical schedule should be established to determine when to change the solder in a wave or drag solder machine.

Heat

The one parameter of soldering that receive the least attention is heat. Heat is defined as a temperature for a time. The objective to obtaining high quality soldering is to have the molten solder contact the metal surface for 1-2 seconds. A longer amount of time may result in excessively thick intermetallic formation and solder joint embrittlement. A shorter amount of time may result in a weak, partial solder bond. To get the proper amount of heat with hand soldering irons, the mass of the tip must be balanced with the mass of the solder joint so that rapid heat transfer can take place. The soldering iron tip temperature should be selected so that each connection can be completed in 1-2 seconds.

With wave or drag soldering automatic machines, the circuit board assembly must be preheated prior to running it across the melted solder. The liquid flux contains alcohol which will boil if it comes into contact with the solder. The preheated will evaporate the alcohol and activate the flux for better cleaning. The rosin fluxes are best preheated to 100-120 C for maximum efficiency prior to wave or drag soldering. This also minimizes explosions by flux on the solder and reduces thermal shock on components and the circuit board.

If the soldering process is going to be a reliable method for joining metals, many factors go into making up the total soldering system. The cost of building electronic assemblies with maximum productivity and quality relates directly to the basic factors for reliable soldering -

solderable metal
surfaces in a solderable configuration
Proper soldering alloy
Correct solder alloy
Sufficient heat

If good controls are maintained on the total system, soldering will become a reliable, efficient method for joining metals rather than a costly, time-consuming, difficult production problem.

Solderpaste and Viscosity

Viscosity and solderpaste is one of the most mis-understood aspects of this new and very important part of "Surface Mount Technology". The problem is that viscosity has very little, if any, bearing on how a solderpaste will actually perform in production.

Viscosity is defined as "the ability of a fluid to resist a force put upon it". We normally think of viscosity as thickness, but, it is more than that. Any fluid material can have an infinite number of viscosities. The reason for this is because a fluids ability to resist force changes with temperature, the strength of the force, the length of time since the force was applied, the phase of the moon, and the average length of one's patience.

It is for this reason, we must be absolutely sure viscosities are always measured with the same piece of equipment and under the exact same conditions. This has proven to be difficult since a lot of people have a tendency to create their own special viscosity test method. These methods may or may not always give results that are meaningful when dealing with solderpaste.

The Kester Solder data sheet supplement outlines our standard method of viscosity measurement. While we prefer to use this method, we do perform special tests for individual customers. In fact, the current count stands at 15 different methods for measuring viscosity. So much for industry standards!

There are three important things to remember:

Viscosity readings are not a very good indication of how a solderpaste will work (screen print, place, reflow, and clean). Two different solderpastes with the same viscosities can perform entirely different, particularly if they have different metal content or are made by different manufacturers. Viscosity measurements are only useful as a very crude method of guaranteeing consistency (i.e., a confidence builder).

If you hold these truths to be self evident, as I do, then an entirely different outlook on viscosity specifications will begin to take shape. While I have an inner confidence and knowledge that viscosity measurements are a convenient placebo, the user is faced with a slightly different reality.

He wonders how he can tell that the manufacturer is telling him the truth, and how is he going to be sure that he is getting good solderpaste. The easiest and most readily available piece of equipment is the Brookfield Viscometer.

The best explanation of why solderpaste viscosity is a useless measurement goes something like this:

Picture taking a Brookfield viscosity measurement. Carefully unseal the jar of solderpaste, which has been sitting in a constant temperature bath overnight (to guarantee the contents are exactly at 25 C). Stir the contents ever so gently so as not to cause unnecessary friction which would heat up the paste or entrap air. Clean off the spindle and set the depth to which the heliopath stand will cause the spindle to travel within the sample. Set the speed at the specified **value** and let it go. In doing this, a curve of values will be obtained which will vary by about 15% from the top of the jar of solderpaste to the bottom. This is all right, however, because we can easily calculate an average **value** which we will call the viscosity.

Now visualize what happens when one stencil prints that same solderpaste at room temperature (whatever that happens to be). The jar is opened, an unspecified amount of solderpaste is dropped onto the stencil, then the squeegee begins to beat the solderpaste back and forth. Invariable, this beating back and forth heats up the solderpaste causing it to thin out. The amount of heating and thinning is determined by the speed at which the squeegee travels and the time between strokes.

Complicate things even further by having the process occur over the course of an entire day with assured solvent evaporation and moisture absorption, etc. Would it not be more sensible to try to produce a solderpaste which will have repeatable stenciling properties, rather than one which will have the same Brookfield viscosity measurement? Believe it or not, it is much easier to make a solderpaste formula perform consistently than to come up with the exact same viscosity. This is because, when we make the paste, we combine the exact same chemicals every time. It only changes slightly because of the environment it was made in, the condition it was stored in, and the methods of preparation for testing. When we start beating the paste with a squeegee, all of those small environmental concerns become insignificant in comparison to the stenciling process.

Looking at it from another angle, what similarity is there between a small piece of stainless steel (the spindle) rotating and going up and down

in a jar of solderpaste and a rubber squeegee constantly pushing it back and forth? It would take hours for the spindle to impart the same amount of energy to the solderpaste as a squeegee does in one single pass. Each system comes to some kind of equilibrium, but they are only remotely related. Better methods of characterizing a solderpaste exist, but unfortunately, the equipment required is cost prohibitive for the average solderpaste user (or manufacturer). Even with the newer cones and plate type viscometer, it is difficult, if not as impossible, to correlate viscosity values with printing performance. Incidentally, a stripped down version of these viscometers usually runs in the range of $50,000.00.

SMT Process Recommendations Defect Minimization Methods for a No-Clean SMT Process

Key competitive advantages can be obtained through the minimization of process defects and disruptions. In today's electronic manufacturing processes there are many variables to optimize. By gaining an understanding of what the defects are, and where they come from, is a key step in the process towards defect free/six sigma manufacturing. In the last decade, Surface Mount Technology processes have been slowly converting towards the No-Clean philosophy. This new trend has spawned new processing issues which need to be addressed. This paper will investigate solutions to current problems in the processing of No-Clean SMT processes. These solutions will be critical in the development of successful processes in the electronics industry in the years ahead.

Introduction:

This paper will discuss commonly experienced defects associated with No-Clean surface mount processes and propose methods to solve these issues. Much of the discussion can be applied to any surface mount process (i.e. water soluble, RMA, or No-Clean), but some are directly associated with No-Clean processes. Some of these defects are due to inefficient reflow profiles - examples of these defects would include cold solder joints, non-wetting, solder balling, and tombstoning.

Other defects can be primarily attributed to the solder paste printing process - these would include insufficient solder joints, bridging, and solder balling; while others can be attributed to miscellaneous process variables - these would include skewed components, solder beading, and solder balling.

The effects of extreme temperature and humidity conditions will also be discussed in this paper. In addition to this, some processing tricks that are designed to maximize the solder paste performance will also be discussed.

Reflow Related Issues:

1. Cold Solder Joint (dull joint): is defined as solder connections exhibiting poor wetting and possessing a grayish, porous appearance after soldering. This is a phenomena that can be associated with all processes.

One cause of this would be insufficient heat present to reflow the solder adequately. It may also be due to the flux's inability to accomplish the soldering task. This may be linked to inadequate cleaning of the component and PCB pads prior to soldering, or it may simply be due to excessive impurities in the solder solution. Possible solutions to this problem include I) raising the maximum reflow temperature high enough to reflow the material thoroughly, 2) preventing vibration of assembly during and immediately after reflow, 3) accelerating the cool down rate after reflow, and 4) checking the alloy **analysis** for high levels of contaminants.

2. Non-wetting: is defined as a condition whereby a surface has contacted molten solder, but has had part or none of the solder adhere to it. Again, this is a phenomena that can be associated to all processes.

There are various causes of non-wetting. It could be due to the base metal being visible, and since this is typically more difficult to solder to, non-wetting occurs. It might also be due to too long of a soak time in the reflow process using up the flux prior to soldering. The flux being used may be ineffective from an activity standpoint. Or, it could possibly

be due to insufficient heat during the reflow process where the flux doesn't see the correct activation temperature.

Therefore, the solutions include 1) rectifying the situation with the PCB manufacturer if the base metal is present, 2) reducing the total profiling time prior to the reflow stage, or following the recommended reflow profile (see Exhibit #1: No-Clean Solder Paste Reflow Profile), and 3) increasing the flux activity, or using the correct flux for the given soldering task (see Exhibit #2: Metal Solderability Cross Reference Chart).

3. Solder Balling: is defined as the formation of very small spherical particles of solder separating from the main body of solder which forms the joint. This is a primary concern for No-Clean processes since a large number of solder balls can create an artificial bridge between two adjacent leads causing functional problems to the electrical circuit. Solder balling is not as big of a concern with water soluble processes since they typically are removed during the cleaning process.

One possible cause of solder balling may be moisture contaminated solder paste. The moisture splatters during reflow leaving solder spheres behind. An improper reflow profile can also cause solder balling. The temperature ramp rate is commonly too high which increases the probability of paste splattering. Solder balling can possibly be due to excessive oxides on the solder powder in the solder paste which inhibits solder coalescence during reflow.

Among the ways to approach this problem are the following 1) select a reflow process which best fits the paste selected (see Exhibit #1: No-Clean Solder Paste Reflow Profile), 2) minimize solder paste's exposure to high temperatures and humidities whenever possible.

4. Tombstoning: is defined as a soldering defect in which a chip component has pulled into a vertical or near vertical position with only one termination soldered to the PCB, resulting from force imbalances during the reflow soldering process. This is also known as drawbridging, the manhattan effect, and the stonehenge effect.

Tombstoning can be caused by uneven heating causing a differential across the component terminals. In other words, the solder melts at different rates and one side reflows before the other forcing the other lead to stand upright. The solderability between two terminations of the component or PCB pads can also be blamed. Uneven paste deposition on the two solder pads has also yielded tombstoning defects. Insufficient tack force of the solder paste to hold the component in place during reflow can also be a factor, but this is typically due to temperature and humidity effects on the solder paste. Excess movement during and after the reflow operation can cause component misalignment which results in tombstoning, and inadequate placement force to make intimate contact between the paste and the termination of the pads can also be a cause.

Solutions to this surface mount defect include 1) increasing he preheating temperature (following the recommended guidelines) so that the temperature differential between the two terminations is low at the time of reflow, 2) selecting components and PCBs with consistently solderable leads and pads, 3) ensuring consistent solder paste deposit heights between pads via a vision system designed to measure solder paste deposition height, 4) avoiding inefficient tack force by avoiding extreme environmental conditions, 5) minimizing the amount of movement the assembly sees during reflow, and 6) increasing component placement force to ensure contact of the component terminal to the solder paste deposit (not too much because bridging may occur if it is too high).

Recommended Reflow Profile:

The majority of no-clean solder pastes are rosin or resin based, and therefore can withstand the traditional reflow profiles used on RMA based fluxes. The goal of the reflow process is to melt the powder particles in the solder paste, wet the surfaces being joined together, and solidify the solder to create a strong metallurgical bond. The profile can be broken down into four zones - the preheat, soak, reflow, and cool down zones. An illustration of this profile can be found in Exhibit #1 at the end of this

paper.

This profile should be used in order to avoid the following process problems. The Pre-Heat section helps prevent against insufficient solvent evaporation, component/PCB shock, and solder ball formation due to splattering. The Soak section guidelines prevent insufficient flux activation and excess oxide formation. And the Reflow section guidelines avoid flux entrapment, void formation, flux discoloration, and component and board damage.

Printer Related Issues:

1. Electrical Opens (due to insufficient solder joints): can be defined as the result of two electrically connected points becoming separated, or as an area on the PCB which interrupts the intended design on the circuit.

Causes for this type of defect are commonly attributed to the solder paste printing stage of a surface mount process. However, other non-printer related factors can also cause electrical opens. Solder paste can clog in the apertures of the stencil, never being released to the PCB pad. This will create an insufficient solder joint due to insufficient solder being placed prior to reflow. Component lead coplanarity (the distance between the PCB pad and the component lead) can also contribute to opens. The solder volume maybe adequate, but if it is not in contact with both the lead and the pad during reflow, an open will occur. Finally, opens may also be a function of the PCB fabrication process itself.

Solutions for electrical opens include 1) correcting the aspect ratio. If solder paste is clogging the apertures it may be due to the aspect ratio being to small. The aspect ratio is defined as the ratio of aperture width to stencil thickness - use a ratio of 2.0 as a guideline for fine pitch applications. 2) Avoid solder paste contamination by avoiding extreme environmental effects in the manufacturing process, 3) investigate lead coplanarity issues and monitor operator material handling procedures, and 4) investigate fabrication issues with PCB supplier.

2. Electrical Bridges (excess solder): are defined as solder that 'bridges' across two conductors that should not be electrically connected, causing an electrical short.

Bridging can be caused by a variety of factors, but they are most commonly caused by problems in the solder paste printing process. The print alignment, or the alignment of the stencil to the PCB pad design, may be slightly off. Bridging can also be caused from too much solder paste being deposited. This may be due to the stencil aperture to pad ratio being too high (1 to 1 for example, where the stencil aperture and the PUB pad have the exact same dimension). Solder paste cold slump can also lead to bridging. Slump is typically a problem if the incorrect solder paste metal to flux weight ratio is being used. High temperatures and humidities can also lead to solder paste slump. Typically, however, if the solder paste includes a thixotropic thickening agent within the flux formula the solder paste will maintain its shape. The reflow profile may also contribute to bridging if the pre-heat section has too slow of a ramp rate. And finally, component contact with solder paste deposit may skew the deposit causing t he solder paste to bridge.

Bridging can be avoided by doing the following 1) use the appropriate solder paste metal to flux weight ratio for the appropriate application. Typically either a higher viscosity or a higher metal content can solve the problem (i.e. dispensable solder paste has a metal content of 85-87% metal typically, this material will slump if used to print fine pitch surface mount. Typically 90% metal is used for a stencil printing solder paste application). 2) Use the appropriate reflow profile (see Exhibit #2), 3) ensure paste deposition is in good resolution and quality without slump or smear prior to reflow (this can be done manually or with an automated vision system), 3) pay close attention to alignment of stencil apertures to pads (automatic printer alignment will alleviate this issue), 4) reduce stencil aperture dimensions by 10% or reduce the thickness of the stencil to reduce the amount of solder paste being deposited, and 5) ensure proper

pressure and accuracy for component placement.

3. Solder Balling: was defined earlier, but it can also be attributed to problems with the solder paste printing process.

Solder balling can be caused by poor solder paste printing alignment where solder paste is printed on the solder mask instead of the pad. The solder paste may not be able to coalesce into the joint and may solidify across two adjacent pads causing a undesirable bridge. Solder paste may also get smeared on the bottom side of the stencil during the printing process.

Solutions to these problems include 1) verifying print alignment prior to reflow on a consistent basis (this can be done manually or automatically via an electronic vision system), and 2) ensuring frequent cleaning of the bottom of stencil (this can be done automatically on automatic printers or manually with a lint free cloth and alcohol).

Miscellaneous Issues

1. Skewed Components (components falling off the pads) can be defined as a descriptive term used to describe the misalignment of an item to its target.

The reasons for the occurrence of this defect are much more straight forward. Insufficient tack characteristics of the solder paste, typically a by-product of extreme temperature and humidity effects on solder paste, is the primary reason for this. Component placement inaccuracies, as well as too much movement of the assembly prior and during reflow, can also contribute to this problem. Poor component or PCB solderability characteristics may also create skewed components.

These problems can be avoided by trying the following 1) abide by recommended temperature and humidity requirements, 2) improve the accuracy of component placement, 3) minimize the amount of movement the unreflowed assembly sees, and 4) improve the solderability of the components or PCBs (this may also be accomplished by using a more aggressive flux).

2. Solder Beading (or Side Balls): is defined as the formation of larger solder balls located near discrete components possessing very low standoff distances.

This defect is similar to solder balling, but it is distinctive in the fact that these solder beads adhere to discrete components as opposed to multi-leaded devices.

The majority of this type of problem is due to excessive amount of solder being deposited. Another reason may be the flux outgassing which overrides the paste's cohesive (coalescence) force during the preheat stage. Component placement pressure may also be too high. Excessive pressure may push deposited solder paste out onto the solder mask where it can not coalesce back into the joint.

Solving this defect can be easily accomplished by doing one of the following 1) reducing the stencil thickness or reducing the aperture dimensions (a 10% reduction on the side where the solder bead occurs should solve this problem), 2) using the recommended temperature profiling guidelines, and 3) reducing the component pick and place pressure.

3. Solder Balling: can also be attributed to the solder paste. Solder balling can occur if the solder paste contains a large percentage of ultra fine powder particles (sub 25 micron in diameter) which can be carried away from the main solder pool by flux during heating. It may also be found that misprinted boards, inadequately cleaned prior to reprocessing, will have solder balls.

If these are the reasons that solder ball formation is occurring, then the following two solutions will help 1) monitor solder paste vendors control of oxide and fine particles in their powder distributions, and 2) use an automated cleaning system to clean misprinted board with an approved solvent (IPA is commonly used).

Temperature/Humidity Effects

Solder paste printing performance, tack life, and reflow characteristics can be greatly affected by the temperature and humidity characteristies of the manufacturing environment. The recommended

temperature the solder paste should be at when printing is 70-77 F. The recommended humidity is between 35-65% RH. Ideal temperature storage for solder paste is typically 0-5 C (32-40 F), but some newer formulas do not require refrigeration (it actually makes the solder paste perform poorly).

If the solder paste is too hot due to the working environment, paste slump is more likely to occur. As discussed previously, this can lead to bridging and other defects. Print definition is also commonly affected and this may lead to solder ball or solder bead formation.

If the solder paste is too cold due to the working environment, the solder paste may become too thick to yield good print definition. This may lead to stencil aperture clogging which in turn will result in insufficient or open joints.

If the solder paste is exposed to extreme high or low humidity, similar problems will result.

Tricks to Extend Stencil Life

Stencil life can be lengthened by using a continuous replacement method for keeping the solder paste in a fresh condition. By simply adding new paste to the stencil as you use it, you can lengthen the life of the paste without degradation of tack or reflow characteristics.

Solder paste volume on the stencil also has a relationship to how long the solder paste will last. It is recommended to have adequate solder paste volume on the stencil so that a 1/4 to 1/2" roll of solder paste is in front of the squeegee at all times. This volume leads to better print definition as well.

The effects of time on reflow and tack characteristics for solder paste that has been printed on a PCB are greatly influenced by the environmental conditions of the manufacturing facility.

The general recommendation is to keep the time between printing and reflow down to a minimum so solderability characteristics are not sacrificed.

World Logic IC Market
1997-2003

Sales ($B)	24.9	34.6	67.6
Units(M)	466.9	648.2	1261.4
Year	1997	1999	2003

World Logic IC Market
By Package Type
1997-2003
Units (M)

SO	140.1	157.5	201.1
QFP	116.7	131.3	167.6
PGA	65.4	81.9	129.8
IP	70.0	54.5	47.4
BGA	35.0	69.5	304.7
DCA	28.0	49.2	147.8
CSP	11.7	104.4	263.0
Total	466.9	648.3	1261.4
Year	1997	1999	2003

World Logic IC Market By Package Type
1996-2003
Units (M)

8 - 32	70.0	78.8	100.6
32 - 132	186.8	210.0	268.1
132 - 180	116.7	178.7	422.6
280 - 400	70.0	117.7	335.2
400	23.3	63.1	134.9
Total	466.8	648.3	1261.4
Year	1997	1999	2003

Publisher Name: New Insights
Industry Names: BUSN (Any type of business); ELEC (Electronics)

33/9/5 (Item 5 from file: 636)
03337189 **Supplier Number:** 46858935

United Kingdom: ASB discusses tangible fixed assets
World Accounting Report , p N/A
Nov 1 , 1996
ISSN: 0243-3303
Language: English **Record Type:** Fulltext
Document Type: Newsletter ; Trade
Word Count: 222
Text:

The Accounting Standards Board (ASB) has published a Discussion Paper (DP) setting out its views on the initial measurement, **valuation** and depreciation of tangible fixed assets. The DP is the first stage towards the development of a new accounting standard on the subject and after comments are analysed the ASB will publish an Exposure Draft as a precursor to a **Financial** Reporting Standard.

ASB chairman Sir David Tweedie, said: 'If accounts are to be meaningful the accounting treatment of tangible fixed assets must be based on firm foundations. Some developments in recent years have undermined these foundations and the DP's proposals aim to put things right.'

Companies that revalued their properties in the late 1980s at the height of the property boom have since been able to leave those valuations in their accounts unchanged. Tweedie said: 'There is no logic in departing from a **historical** cost system simply to inject **random** revaluations of assets at irregular **intervals**.'

The DP argues that the present unclear position on the capitalisation of interest should be resolved and that in future capitalisation should either be mandatory or be prohibited. The DP also discusses whether investment properties should continue to be exempt from depreciation and concludes that the exemption should continue to apply. Comments are invited by early next year.

Publisher Name: Financial Times Group
Industry Names: BANK (Banking, **Finance** and Accounting); BUSN (Any type of business); INTL (Business, International)

33/9/6 (Item 6 from file: 621)
01365584 **Supplier Number:** 46281601
Computron introduces Sentinel, the first real-time Workflow process monitor.

Business Wire , p 4041158
April 4 , 1996
Language: English **Record Type:** Fulltext
Document Type: Newswire ; Trade
Word Count: 1036
Text:
RUTHERFORD, N.J.--(BUSINESS WIRE)--April 4, 1996--Computron Software Inc. (Nasdaq: CTRN) has introduced Computron Sentinel(TM), the software industry's first real-time business process monitoring system for workflow applications.

Sentinel is the latest enhancement to Computron Workflow, an Imaging Magazine Product of the Year, and utilizes Arbor Software Corporation's Essbase OLAP (On-Line Analytical Processing) engine to represent in-process workflows in an innovative multidimensional model.

Workflow software allows users to automate and simplify business processes by defining and automating the rules, roles and routes that are integral to business processes and the people who participate in them. As a result, the workflow system not only simplifies and automates the flow of electronic information from point to point through the enterprise, but also enhances the performance of traditional computer-based tasks. Until now, however, workflow monitoring has consisted of "after-the-fact" reports generated by the workflow system.

"With Computron Sentinel, users of workflow software can monitor business processes as they are performed in much the same way that real-time shop floor systems track manufacturing processes," said Christopher Mauldin, Director of Strategic Planning for Computron Software Inc. "This is a first for workflow users, and it will significantly enhance their ability to closely manage business processes and quickly make day-to-day business decisions with confidence. Computron Sentinel will allow companies to become more proactive in managing their business process environment."

The Computron Sentinel system shows a real-time picture of automated business processes, including:

o What tasks are being performed; o The depth of workflow queues (by task or by individual); o Average cycle times per work item; o Workflow thresholds that are being exceeded.

Workflow thresholds, for instance, can be automatically established based on **historical** trend **analysis**. Computron Sentinel can automatically generate a warning and, if appropriate, trigger a workflow event such as electronic mail notifications to the supervisor. In addition, flashing color changes on the real-time monitor screen alert supervisors to take corrective actions.

Computron Sentinel not only provides real-time workflow tracking, but also allows a graphical review of workflow history. Thus, Sentinel system users can perform a "fast-forward" review of a particular period of time. When exceptions occur -- perhaps graphically represented by a spike in a graph -- users can pause the display and drill down into the workflow database for more information, and they can take corrective action if necessary. Furthermore, Sentinel system provides a rich source of workflow

metrics -- cycle times, occurrences outside of deviations, costing of processes -- all of which can be utilized for process improvement and "what-if" testing in a sophisticated computer simulation system. Computron Sentinel thus becomes a vital information source for resource planning and workload balancing.

Arbor Software's Essbase fills an essential function in the Sentinel system, Mauldin said, "because it stores information in a manner that highly optimizes **random**
 information retrieval and manipulation."
In practice, Essbase receives a complete "snapshot" of workflow system data every few minutes. Then Essbase allows the Sentinel system to extract that up-to-date workflow information for use in a wide range of graphical views, for measurement of precise system metrics, and to trigger automatic workflow "events" such as notifying a supervisor when workloads are imbalanced or predefined thresholds are exceeded.

Using Essbase with Sentinel, users can now perform departmental reporting, marketing **analysis**
, expense **analysis**
, and
customer and product profitability models from information previously locked up in computer-stored images and documents. While reviewing the Essbase reporting model in a spreadsheet, users can "drill down" to the actual stored invoice, purchase order, project notes, or variance explanation directly from Essbase. Essbase polls the workflow system and retrieves statistics at predetermined time **intervals**
, building a
historical
 multidimensional view of all the automated processes.

Computron Sentinel's graphical metaphor, which can be customized by the user, is another key component of its functionality. "Sentinel allows a manager to monitor intuitively what's going on in a business process," Mauldin explained. "And because the system is exception-driven, the manager can make decisions when problems occur, rather than having to search for problems to solve."

Arbor Software Corporation Background Information

Arbor Software Corporation (Nasdaq:ARSW) develops and markets client/server software for business planning, **analysis**
 and
management reporting. Arbor's products are used by more than 650 corporations spanning a broad range of industries and business applications, including Bank of Boston, Emery Worldwide, Fidelity, Los Angeles Times, Neutrogena, Pennzoil, PEPSICO, Prudential and Sears. Arbor has over 80 application, services, tools and platform partners, including Comshare, Hewlett-Packard, IBM and Microsoft. Arbor's products are sold direct, as well as through system integrators and VARs worldwide. Arbor's offices are located in Atlanta, Boston, Chicago, Dallas, Houston, Los Angeles, New York, Sunnyvale, Washington, D.C., and London. More information on Arbor products and services can be found on Arbor's World Wide Web (WWW) site at http://www.arborsoft.com.

Computron Software Inc. Background Information

Headquartered in Rutherford, N.J., Computron Software is an international software company that designs, markets and supports n-tier client/server-based **financial**
, workflow and computer output
on-line (COOL) report/data archiving software solutions that are interoperable across most major UNIX and legacy architectures, as well as on Microsoft Windows NT. Computron was one of the pioneers in the development and integration of high-impact business process reengineering, workflow and COOL technologies into client/server packaged software applications. These technologies add **value**
 by automating
business processes and expanding the role of **financial**

software
from its roots in accounting to encompass literally every person and department enterprise-wide, bringing together all forms and types of information and automating their movement throughout the organization.

Computron currently markets its products and services through a direct sales force and indirect channels throughout the world. The company has 17 offices and distributors in 13 countries in North America, Europe, Asia and Africa. -0- NOTE TO EDITORS: Computron Workflow and Computron Sentinel are trademarks of Computron Software Inc. Essbase is a registered trademark of Arbor Software Corporation. All other companies and product names are trademarks or registered trademarks of their respective companies.

CONTACT: Crescent Communications
Michelle Pujadas, 770/698-8650, ext. 120
Paul McKeon, 770/698-8650, ext. 107
Fax: 770/698-8651
mpujadas@crescomm.com
pmckeon@crescomm.com
or
Computron Software Inc.
Alex Plavocos, 201/935-3400, ext. 676
or
Arbor Software
Joanna McMillan, 408/541-4035
Fax: 408/727-7140
jmcmillan@arborsoft.com

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